

Decoupled High-Mobility Graphene on Cu(111)/Sapphire via Chemical Vapor Deposition

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The growth of high-quality graphene on flat and rigid templates, such as metal thin films on insulating wafers, is regarded as a key enabler for technologies based on 2D materials. In this work, the growth of decoupled graphene is introduced via non-reducing low-pressure chemical vapor deposition (LPCVD) on crystalline Cu(111) films deposited on sapphire. The resulting film is atomically flat, with no detectable cracks or ripples, and lies atop of a thin Cu₂O layer, as confirmed by microscopy, diffraction, and spectroscopy analyses. Post-growth treatment of the partially decoupled graphene enables full and uniform oxidation of the interface, greatly simplifying subsequent transfer processes, particularly dry-pick up — a task that proves challenging when dealing with graphene directly synthesized on metallic Cu(111). Electrical transport measurements reveal high carrier mobility at room temperature, exceeding 10⁴ cm² V⁻¹ s⁻¹ on SiO₂/Si and 10⁵ cm² V⁻¹ s⁻¹ upon encapsulation in hexagonal boron nitride (hBN). The demonstrated growth approach yields exceptional material quality, in line with micro-mechanically exfoliated graphene flakes, and thus paves the way toward large-scale production of pristine graphene suitable for high-performance next-generation applications.

1. Introduction

Graphene offers enticing prospects for a variety of applications ranging from photonics^[1] sensing and optoelectronics^[2] to spintronics^[3] and novel quantum technologies.^[4–6] In all these fields, large-scale highly crystalline graphene is requested to access the outstanding electronic properties that sparked enormous research interest in this material since its early years.^[7] Specifically, graphene-based quantum technologies include known elements, such as quantum dots,^[8,9] transmons^[10,11] and single-photon bolometers,^[12,13] as well as entirely novel paradigms, such as moiré quantum simulators^[14] and topological qubits based on superconducting proximity in the quantum Hall (QH) regime.^[15–18] The latter approaches, being based on correlated electronic phases, require extremely clean material platforms. To date, the gold standard for studies in

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this realm is represented by exfoliated graphene flakes encapsulated in between hexagonal boron nitride (hBN) crystals.^[19] However, it has become clear that the development of scalable methods for graphene synthesis and transfer is crucial for the realistic adoption of these highly demanding graphene-based technologies.

Graphene synthesis via chemical vapor deposition (CVD) on copper (Cu) foils has been shown to yield graphene single crystals of hundreds of micrometers lateral size that, once encapsulated with hBN, display state-of-the-art transport properties comparable to those of exfoliated graphene flakes^[20–23] (see Table S1, Supporting Information). Yet, Cu foils have a polycrystalline nature and the continuous graphene films obtained on top consequently present different crystallographic orientations and grain boundaries which are detrimental to electronic transport.^[24] To solve this issue, complete conversion of polycrystalline Cu foils into Cu(111) via annealing in hydrogen (H₂) atmosphere has been developed.^[25] However, the non-rigid nature of the foils and the resulting micrometer-scale surface-height variations lead to poor temperature control over millimeter-scale areas during graphene growth and to non-homogenous graphene quality across wafer-scale dimensions. The use of a rigid template is required in most fab-scale scenarios (i.e., CMOS lines), where the adoption of foils can be hardly envisioned, due to the difficulty of handling and lack of control for Cu source materials. For all these reasons, significant efforts have been devoted to developing graphene growth on crystallographically oriented rigid Cu substrates such as Cu single crystals, either bulk or deposited on carrier wafers.^[26–29] Among the different possible Cu orientations, Cu(111) is isomorphic to graphene (with a $\approx 3.8\%$ lattice mismatch), making it the preferential orientation for the growth of high-quality graphene crystals.^[30–35] Cu(111) obtained by epitaxial deposition of Cu films on crystalline substrates such as c-plane sapphire^[27,29–31,36–39] offers appealing features, such as surface flatness, the possibility of setting the film thickness, and the ease of controlling film orientation guided by the underlying substrate crystal structure.^[40] Yet, when graphene is synthesized on Cu(111) films, its dry transfer is extremely challenging due to low Cu(111) oxidation rates.^[41–44] Indeed, Cu oxidation is instrumental for successful graphene transfer, as the oxidation process weakens the interaction between Cu and graphene, thus facilitating the delamination of graphene with minimum induced damage.^[20] Yet, the strong Cu(111)/graphene coupling^[45] and the inferior propensity to oxidation of Cu(111) (with respect to that of Cu(110) and Cu(100))^[42] make oxidation of such samples not trivial. Recently, it has been demonstrated that atomically flat Cu(111) surfaces with monoatomic step edges are resistant to oxidation for over 1 year.^[46] In essence, while high-quality graphene can be grown on Cu(111) films, its transfer, especially via dry pick-up technique, is problematic. To date, electrical transport results approaching those reported for graphene grown on Cu foil have been achieved only on the non-trivial high-index Cu orientation (168) obtained on MgO substrates^[42] (see Table S1, Supporting Information).

Here, we unveil that Cu(111) evaporated on c-plane sapphire indeed serves as a suitable platform for both growth and subsequent clean transfer of graphene yielding electrical transport performance comparable to that of exfoliated flakes. We show that by substituting the process gas used in the pre-growth anneal-

ing step from reducing H₂ to non-reducing Ar and by using a confined oxygen-rich environment, low-pressure CVD (LPCVD) can be used to synthesize high-quality graphene, which is decoupled from the Cu(111) growth substrate and can be easily delaminated. The graphene obtained in this way shows a preferential crystallographic orientation and the copper film is particularly flat with a roughness in the sub-nanometer range. Low energy electron diffraction (LEED), high-resolution scanning transmission electron microscopy (HR STEM), X-ray photoelectron spectroscopy (XPS), and angle-resolved photoelectron spectroscopy (ARPES) analyses demonstrate that graphene grows atop a thin superficial layer of Cu₂O(111), instead of bare Cu(111). The high quality of the synthesized material is proved by both Raman fingerprints (indicating reduced strain fluctuations and low doping level) and by room-temperature mobility on SiO₂/Si as high as $\approx 11\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $n = 1 \times 10^{12}\text{ cm}^{-2}$. Post-growth treatment of the samples in an environmental chamber leads to a fully oxidized interface, enabling the hBN-mediated dry pick-up of graphene from Cu(111), and the fabrication of ultra-high-quality transport devices (room-temperature mobility $\approx 75\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $n = 1 \times 10^{12}\text{ cm}^{-2}$, see Table S1, Supporting Information). These results indicate weakly-coupled graphene grown on Cu(111) as the ideal candidate for the scalable synthesis of flake-grade graphene and a platform for the development of novel technologies based on 2D materials.

2. Results and Discussion

2.1. Growth of Decoupled Graphene on Cu(111)/Sapphire

Graphene was grown by LPCVD on $\approx 3\text{ }\mu\text{m}$ Cu film thermally evaporated on c-plane sapphire as described in the *Methods* section. Before Cu evaporation, the sapphire was subjected to chemical treatment in Piranha solution to ensure surface termination with -OH groups,^[36,47] which allowed us to obtain single-crystal Cu(111) (Figure S1a, Supporting Information). **Figure 1a** shows a side profile and a schematic illustration of the Cu film/sapphire configuration during the graphene growth process. Briefly, the Cu/sapphire substrate (illustrated with a partial cutaway to reveal the configuration below) was placed with the Cu film facing down toward a supporting sapphire dice at a distance of $\approx 0.4\text{ mm}$. Four pieces of sapphire were used as pillars to separate the growth substrate from the support sapphire so that the Cu film was held at a temperature $\approx 40\text{ }^\circ\text{C}$ lower than that of the bottom graphite heater (Figure S2, Supporting Information).^[27] With this arrangement, we created a confined reaction space which has been shown to create a uniform reactant concentration distribution^[48,49] and to improve the substrate morphology.^[49,50] In our process, we substitute the conventional H₂ annealing step, typically performed on Cu to increase grain size and promote Cu(111) crystallization,^[25] with non-reducing Ar annealing, preserving the native oxide present on the Cu thin film. Furthermore, Xu et al. demonstrated that the sapphire support acts as an additional source of oxygen during the growth processes.^[51] Oxygen is known to play several roles during graphene growth, such as reducing defect density,^[51–55] and increasing growth rate.^[51]

Figure 1b shows an optical microscopy image of as-grown isolated graphene crystals on Cu film/sapphire. To discern the growth orientation of graphene, we intentionally limited the

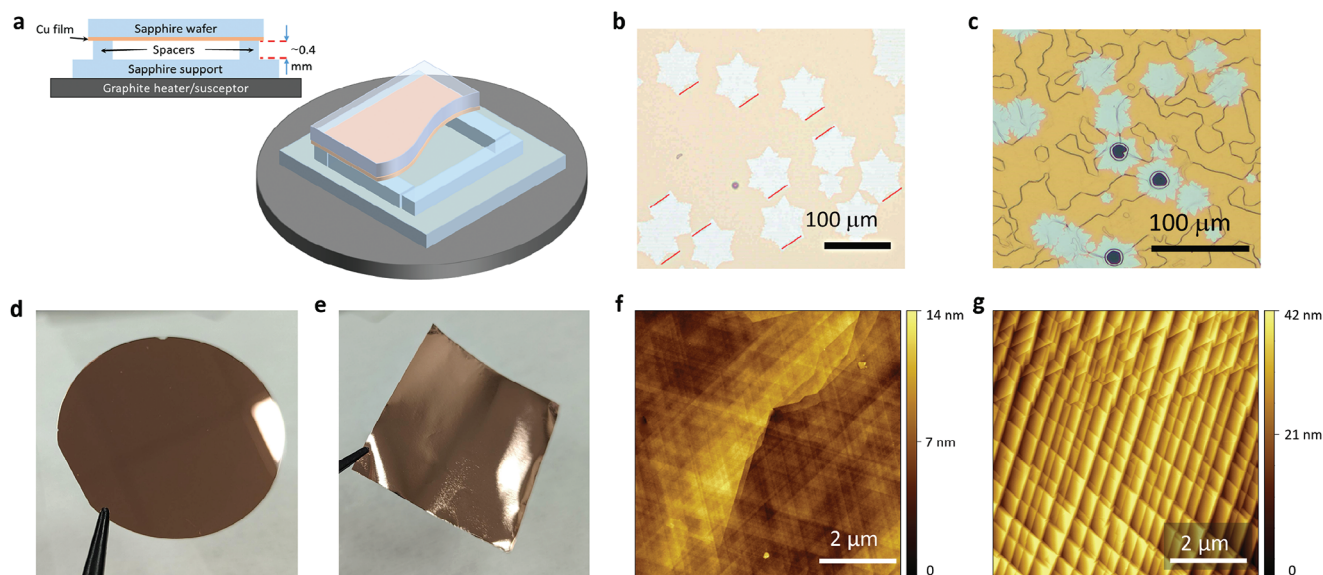


Figure 1. Microscopic characterization of as-grown graphene. a) Schematic cutaway illustration of graphene sample configuration during LPCVD, showing the Cu film deposited on sapphire, sapphire pillars ensuring a gap between the Cu film and the support sapphire, and the sapphire support lying on graphite heater. b) Optical image of isolated graphene crystals on Cu film grown in a confined configuration, showing a single orientation. c) Optical image of graphene on Cu film/sapphire grown without confinement. d) Picture of a 2" sapphire wafer with evaporated Cu. e) Picture of a commercial Cu foil. f) A typical AFM image of as-grown graphene on Cu film/sapphire with measured average roughness $R_q \approx 0.6$ nm and g) graphene on Cu foil with $R_q \approx 5.4$ nm over $2 \times 2 \mu\text{m}^2$.

growth time to 15 min and obtained isolated crystals. The graphene crystals mainly share the same orientation, as inferred from the aligned hexagonal shapes (see red lines in Figure 1b). By increasing the growth time to 25 min, the crystals seamlessly merged into a continuous monolayer graphene film^[56] with uniform morphology (Figure S3a,b, Supporting Information). Crucially, in both cases the Cu film appears to be free of grain boundaries, twinning, and dewetting, unlike the Cu film treated in unconfined geometry (Figure 1c; Figure S4, Supporting Information), proving the role of partial enclosure in mitigating Cu sublimation during LPCVD.

To evaluate the roughness of the as-grown graphene on Cu film/sapphire, surface topography was investigated using atomic force microscopy (AFM). Figure 1f,g show AFM micrographs of graphene grown under similar reactor conditions on Cu film (Figure 1d) and on Cu foil (Figure 1e), respectively. The measured root mean square (RMS) roughness (R_q) value of the graphene/Cu film/sapphire over a $2 \times 2 \mu\text{m}^2$ area is ≈ 0.6 nm. Upon graphene growth, the Cu film displays 60° mutually oriented steps of ≈ 0.5 nm height due to dislocations, caused by the lattice misfit between Cu and sapphire (Figure 1f; Figure S3c,d,f, Supporting Information). In some locations, step bunching with heights up to 2 nm is visible (center of AFM micrograph in Figure 1f; Figure S3c,e, Supporting Information). In all instances, the surface is atomically flat within the observed terraces. In contrast, the morphology of the graphene/Cu foil surface is much rougher, in agreement with previous reports.^[27] The R_q value for graphene on Cu foil across a $2 \times 2 \mu\text{m}^2$ region is ≈ 5.4 nm. These observations indicate that our approach successfully provides an ultra-flat Cu film morphology for the growth of graphene, which in turn presents no signs of cracks, wrinkles, or ripples. We ascribe the flatness of our film to the confinement-

driven suppression of Cu sublimation during growth, as previously demonstrated in enclosure growth approaches on Cu foils.^[27,49,57]

The structural, chemical, and electronic properties of the graphene synthesized on Cu after Ar annealing were investigated via LEED, HR STEM, XPS, and ARPES. Notably, LEED performed on continuous graphene films immediately after growth reveals a complex diffraction pattern. In Figure 2a we can see that at 67 eV, electron diffraction reveals the presence of graphene (outermost ring), together with Cu(111) spots, the brightness and sharpness of which indicates an optimal ordering of the substrate. In addition, we observe a pattern that we attribute to Cu_2O , aligned with the Cu(111) registry and indicated by the orange circle. The pattern exhibits an additional feature, which we label with a green circle and that we assign to an oxygen-deficient ($\sqrt{3} \times \sqrt{3}$) $R30^\circ$ reconstruction of the Cu_2O .^[58] XPS analyses confirm the presence of a thin oxide layer underneath graphene.^[59] Angle-dependent XPS was performed on the Cu Auger LMM transition and O1s core level (Figure 2b; Figure S5, Supporting Information, respectively). This analysis provides insights into the depth distribution of each component. At high emission angles, bulk components experience higher damping as the effective electron path becomes longer, in favor of the most superficial layers. As it is visible from Figure 2b, the shoulder at lower kinetic energies—assigned to Cu_2O ^[59]—becomes dominant at high emission angles, thus confirming the superficial nature of the Cu_2O . Analyzing the O 1s core level we can discriminate between the bulk Cu_2O component and the interfacial contribution to the photoemission signal (see Figure S5, Supporting Information). Interestingly, non-significant Cu_2O -related fingerprint at 640 cm^{-1} or CuO at 500 cm^{-1} could be detected while performing micro-Raman mapping on similar samples or even

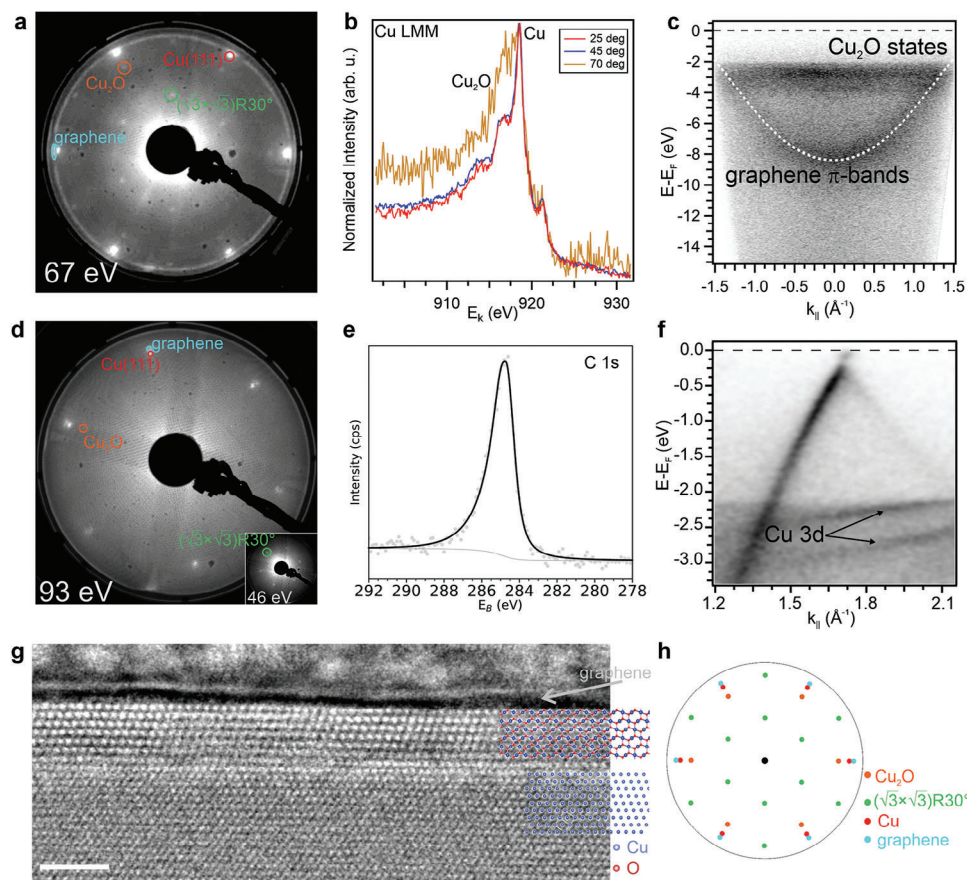


Figure 2. Surface analysis of graphene grown on Cu/sapphire a) LEED pattern recorded at 67 eV on a continuous graphene film showing the pattern of reconstructed $\text{Cu}_2\text{O}(111)$ on $\text{Cu}(111)$, as well as a polycrystalline graphene ring. b) Auger LMM spectrum measured with $\text{Al K}\alpha$ at different emission angles, highlighting the surface nature of the Cu_2O (low kinetic energy shoulder). c) ARPES spectrum recorded in normal emission, showing the states related to the Cu_2O between -0.5 and -4 eV and the graphene π -bands with superimposed NN tight-binding graphene bands. d) LEED pattern recorded on a partial growth at 93 eV. Inset: LEED recorded at 46 eV, where the $(\sqrt{3} \times \sqrt{3})R30^\circ$ pattern is well visible. e) the corresponding C 1s peak, centered at 284.5 eV. f) ARPES spectrum taken at the K-point of graphene along the ΓK direction. g) High-angle annular dark field (HAADF) HR STEM cross-sectional image of the graphene/ Cu_2O /Cu stack, highlighting the atomic positions with a ball-and-stick model placed on the right side. The thickness of the epitaxial Cu_2O layer is 1.6 nm (6 MLs). The imaging zone axis is $[110]$, and the vertical crystallographic direction is $[111]$. The scale bar is 2 nm. h) sketch of the interpretation of the observed LEED patterns.

on the same sample after UHV analysis (Figure S6, Supporting Information), likely indicating that the appearance of these bands is linked to higher oxide levels. ARPES measurements revealed the presence of Cu_2O states, visible as non-dispersive states in Figure 2c, further confirming the presence of Cu_2O at the interface.^[60] Graphene π bands are instead well distinguishable, due to their typical bowl shape, with its minimum centered in Γ . For clarity, we have added nearest neighbor (NN) tight-binding graphene bands to the data (white dashed line). The analysis of a continuous film allows us to exclude the presence of Cu_2O contributions from uncovered Cu regions, which are known to oxidize upon air exposure.^[59,61,62]

Additional surface-sensitive studies were conducted on graphene samples with partial coverage, which were used for magnetotransport measurements. Concerning graphene, LEED revealed a dominant graphene orientation, aligned with the $\text{Cu}(111)$ substrate, indicating iso-oriented graphene crystals (Figure 2d). In addition, also in this case we can observe a weak LEED signature of the $r3$ reconstruction, which we recorded at

46 eV and reported in the inset of the figure. The spots of the Cu_2O are visible as well, although very weak (see inset in panel d). These LEED patterns were different from those measured for samples obtained with the same growth process yet preceded by hydrogen annealing. Indeed, in the H_2 annealing case, as shown in Figure S1b (Supporting Information), a $\text{Cu}(111)$ diffraction pattern and a diffuse graphene diffraction ring were observed.^[63] The C 1s core level peak reported in Figure 2e has been fitted with a single Doniach–Sunjic lineshape centered at 284.5 eV, indicating the good quality of the graphene layer. ARPES measurements offer further insights into the electronic band structure of the system (Figure 2f). The Dirac cone is visible, together with states further below the Fermi level assigned to Cu 3d states.^[64,65] The Dirac point (E_D) is sitting near the Fermi level (E_F) (i.e., within 150 meV), indicating weak coupling with the Cu_2O -terminated substrate (it should be noted that in several instances we find $E_D \cong E_F$). Graphene grown directly on metallic $\text{Cu}(111)$ displays a more prominent interaction with the substrate, compared to what is reported in Figure 2f. This is reflected

in a higher charge transfer from Cu to graphene and a further shifted charge neutrality point at higher binding energies, along with the hybridization of graphene π and Cu 3d bands (Figure S7, Supporting Information).^[63,64] Finally, direct evidence of the presence of a Cu₂O buffer layer is provided by the HAADF-HR STEM analysis reported in Figure 2g. This analysis clearly shows the oxide layer separating the graphene (the darkest, thin layer) from the metallic Cu(111). In agreement with LEED analysis, HR STEM indicates that Cu₂O epitaxially grows as an ordered crystal onto the Cu(111) plane, retaining the substrate's registry and with a thickness varying between a few atomic layers and several nanometers. For clarity, we provide a ball-and-stick model of the crystal structures of both the copper and cuprous oxide crystals on the right side of panel g, while in panel h we show our interpretation of the observed LEED patterns. Further chemical characterization performed by STEM Energy-dispersive X-ray spectroscopy (EDX) is reported in Figure S8 (Supporting Information). Cu₂O act as a decoupling layer so that the interaction with Cu is lessened and further oxidation is facilitated. Upon aging (up to 4 months) in a vacuum desiccator (\approx 5 mbar), XPS and Raman analysis revealed that Ar-annealed samples present a significant oxidation, sensibly higher than that of H₂-annealed ones (Figure S9, Supporting Information). In particular, we noticed that Raman spectra of oxidized Ar-annealed samples revealed a symmetrical spectrum of the G peak, indicating the presence of a uniform graphene-Cu interaction environment, whereas aged H₂-annealed samples presented a G-Peak split, likely revealing inhomogeneous oxidation. It should be mentioned that this is not the first time that graphene growth on thin Cu₂O, a direct bandgap semiconductor^[60] hosting great potential for energy conversion,^[66–68] is reported.^[63,69,70] Our growth configuration, non-reducing Ar annealing, and oxygen-rich experimental conditions allow us to maintain the native Cu₂O layer and enhance its ordering, as explained in the SI.

2.2. Transfer on SiO₂ and Electrical Transport Characterization

Transfer and integration of graphene on technologically relevant substrates, such as SiO₂/Si, SiN, SOI (Silicon on insulator), is imperative for the development of graphene-based photonics, (opto)electronics, sensing but also novel spintronics and quantum applications. In particular, carrier mobilities approaching 10 000 cm² V⁻¹ s⁻¹ are required for several of these applications.^[1] To date, SOTA average mobilities for graphene synthesized on Cu(111) and transferred on SiO₂/Si are in the order of 6000–7000 cm² V⁻¹ s⁻¹.^[26,28] To assess the quality of our material, as-grown graphene was transferred to 285 nm SiO₂/Si substrate using a hybrid method previously developed for graphene on Cu foil,^[71] whereby the graphene layer, attached to polymeric support, is electrochemically delaminated from the growth substrate in 1 M NaOH solution and laminated onto the target substrate in air, minimizing the contamination trapped at the interface. The polymer support was then removed using a two-step cleaning procedure reported in Ref. [72] This approach is known to provide high-quality graphene with low polymer contamination,^[71] with perspective for wafer-scale device application.^[73] Figure 3a shows a schematic representation of a typical electrochemical delamination-based transfer, followed

by dry lamination of graphene onto SiO₂/Si (see Experimental Section for details). This approach was implemented to transfer both single-crystal and chip-scale continuous graphene (see Figure S10, Supporting Information).

As a standard tool to evaluate the quality of electrochemically transferred graphene, we made use of Raman spectroscopy.^[74] Figure 3b shows a representative Raman spectrum, part of a mapping acquisition (150 spectra in total). The spectrum shows the standard fingerprints of high-quality defect-free monolayer graphene: a single-Lorentzian and sharp 2D peak, a large intensity ratio between 2D and G, a negligible defect-induced D peak. For a comprehensive analysis, we fit the spectra from the mapping acquisition with Lorentzian 2D and G peaks, obtaining the following values (average \pm one standard deviation) for the position (Pos) and full width at half maximum (FWHM): Pos(2D) \approx 2672.3 \pm 0.8 cm⁻¹, Pos(G) \approx 1581.7 \pm 0.6 cm⁻¹, FWHM(2D) \approx 22.4 \pm 0.9 cm⁻¹, FWHM(G) \approx 12.5 \pm 1.2 cm⁻¹. It is well accepted that the two peaks are affected by both doping^[75,76] and strain.^[77–79] In Figure 3c–f we show four scatter plots highlighting possible correlations between the fitted peak parameters (the corresponding histograms are presented in Figure S11b, Supporting Information), which are instrumental in discerning the underlying material properties. As shown in Figure 3c, both Pos(2D) and Pos(G) slightly deviate from the accepted intrinsic values for graphene (Pos(G) = 1581.6 cm⁻¹ and Pos(2D) = 2668.9 cm⁻¹ at 532 nm excitation taking into account the dispersion of the 2D peak;^[74] see also Figure S11a, Supporting Information). The correlated Pos(2D)-Pos(G) behavior can be quantified as the slope of the linear fit shown as a red line in Figure 3c, which we find to be 0.84. According to refs. [80,81], this slope value suggests variations in the carrier doping along the crystal as the dominant origin of the Pos(2D)-Pos(G) dispersion,^[75,82–84] with likely minor influence from point-to-point strain variations. Accordingly, in Figure 3d,e, we observe a clear correlation of Pos(G) with both FWHM(G) and the peak area ratio A(2D)/A(G). Despite these variations, based on the values of these parameters, the overall doping level of the graphene crystals likely remains \approx 100 meV.^[75,85,86] Finally, FWHM(2D) uniformly attests to lower values with respect to the typical observations for graphene on SiO₂/Si^[87,88] (Figure 3f), indicating a remarkably low level of strain fluctuations,^[89] which is crucial for the fabrication of high mobility devices.^[87,88] The low level of strain fluctuations can be traced back to the growth of decoupled graphene on Cu(111).^[29,90] Raman maps of the 2D peak FWHM (indicating the nanometric strain variation within the sample) and of the 2D/G peak area ratio (indicating the doping variation) are reported in Figure S12a,b (Supporting Information). Next, we evaluated the electrical transport properties of our electrochemically transferred graphene by measuring standard back-gated Hall bars in four-probe configurations in ambient conditions (see Figure 3g). Figure 3h shows a typical resistance peak as a function of the back-gate voltage (V_{bg}). The charge neutrality point (CNP) at $V_{bg} \approx$ 17.2 V indicates that the graphene is p-doped, which is typical for PMMA-processed graphene measured in ambient conditions,^[91,92] with a doping level consistent with our Raman evaluation. The charge inhomogeneity at the CNP, n^* , was obtained from linear fits of the conductivity as a function of the carrier density on a double-logarithmic scale resulting \approx 1.2 \times 10¹¹ cm⁻² (see the inset in Figure 3h). The carrier density-dependent room temperature

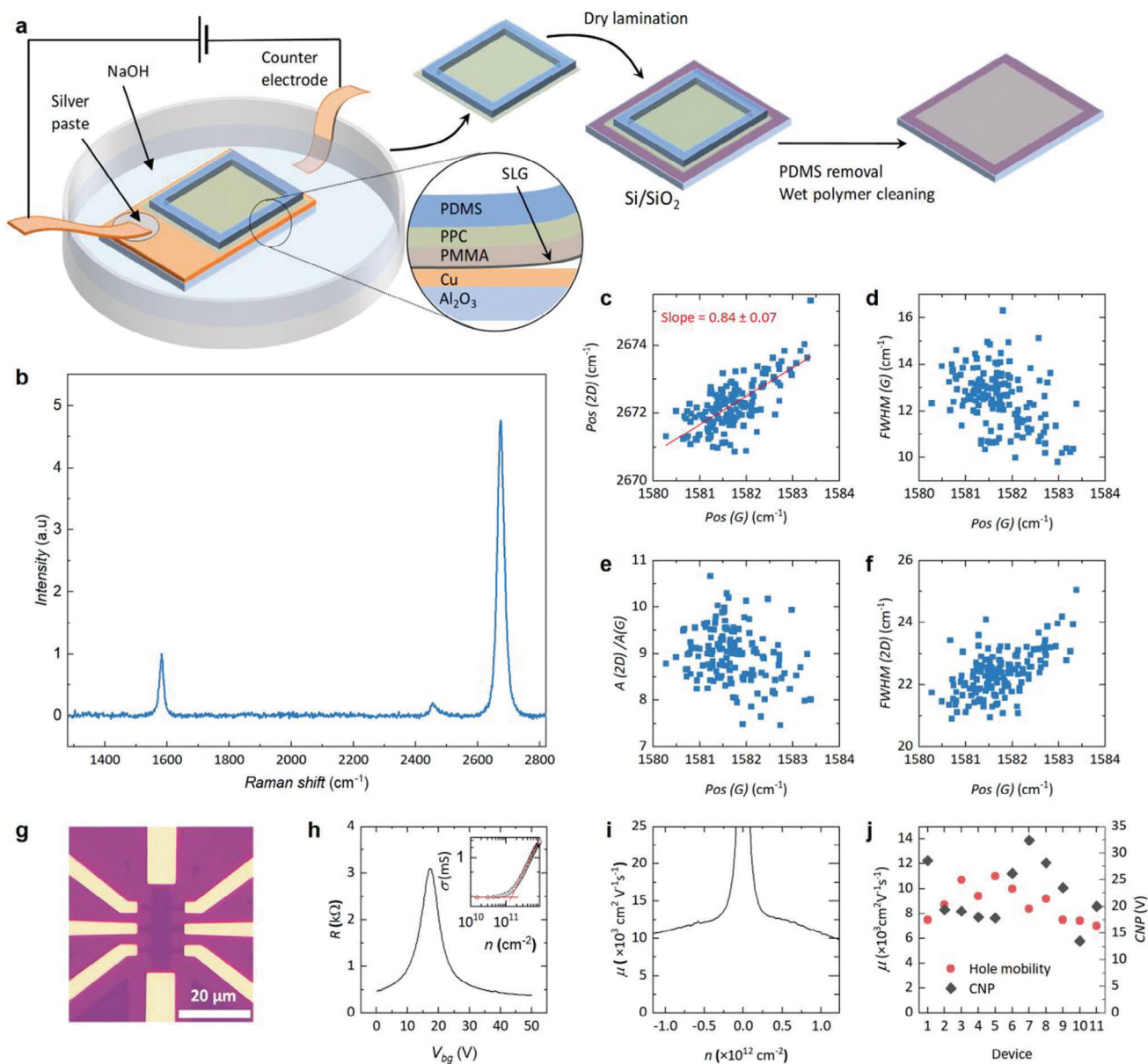


Figure 3. Graphene transfer and characterization. a) Schematic illustration of electrochemical delamination of as-grown graphene and its transfer on the target substrate. The inset shows the material stack: a PPC/PMMA membrane to support graphene and a PDMS frame for handling. The silver paste was used to attach a Cu electrode to the copper film. b) Representative Raman spectrum of the electrochemically transferred graphene. c) Pos(2D) as a function of Pos(G). The red line is a linear fit to the data, with a slope of 0.94. d) FWHM(G) as a function of Pos(G). e) A(2D)/A(G) as a function of Pos(G). f) FWHM(2D) as a function of Pos(G). g) Optical image of a typical graphene Hall bar on SiO₂/Si. h) Resistance as a function of gate voltage measured at room temperature. Inset: linear fit of conductivity as a function of carrier density to estimate the charge inhomogeneity n^* . i) Room temperature mobility as a function of carrier density calculated according to the Drude model from device g. j) Mobility and charge neutrality points for all devices on a chip (11 devices) with average mobility of $\approx 9000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and average CNP of $\approx 22.5 \text{ V}$.

carrier mobility (μ) of a representative device, shown in Figure 3i, was calculated using the Drude formula $\mu = 1/(ne\rho)$, where n is charge carrier density (calculated from V_{bg} using the standard gate lever arm for 285 nm SiO₂), e is electron charge and ρ is the measured resistivity. As shown by the curve, the room temperature hole and electron mobility at $|n| = 1 \times 10^{12} \text{ cm}^{-2}$ is $\mu_h \approx 11000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_e \approx 10000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. Both the μ and n^* values are in line with the highest perform-

ing graphene samples on SiO₂ substrate.^[87] Considering all 11 fabricated devices on a chip, we obtain an average mobility of $\approx 8800 \pm 1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an average CNP of $\approx 22.5 \pm 5.8 \text{ V}$ (Figure 3j) demonstrating that the quality of graphene on a chip is uniformly high, which is crucial for scalable device applications. The demonstration of $\approx 10000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ mobility for CVD graphene grown on a rigid template and transferred to a technologically relevant substrate represents a long-standing goal

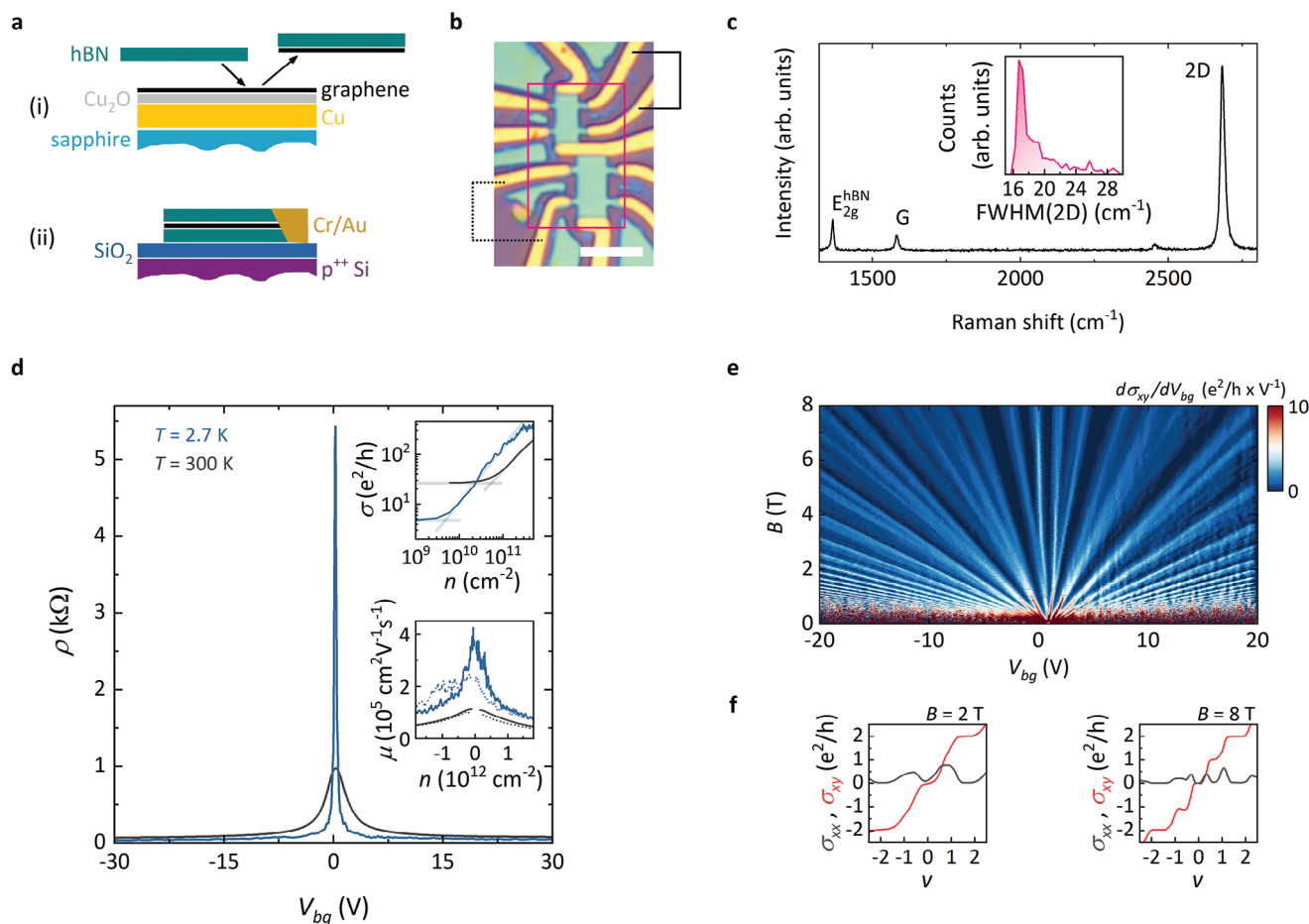


Figure 4. Dry van der Waals pick-up from Cu(111) thin film for ultra-high-quality graphene devices. a) Schematics of the hBN-mediated pick-up and encapsulation: (i) after Cu oxidation in humidified atmosphere, an hBN flake is used to detach a graphene crystal from the growth substrate; (ii) complete encapsulation is finalized using standard dry techniques, followed by device processing. b) optical microscopy image of two Hall bars fabricated following the process depicted in panel a. The pink rectangle indicates the area characterized by scanning micro-Raman spectroscopy prior to processing (see panel c). The continuous and dotted lines identify the contacts used for transport measurements. Scale bar: 5 μm . c) representative Raman spectrum of the vdW stack shown in panel b. Inset: statistical distribution of the FWHM(2D) measured over the pink rectangle in panel b (384 spectra). d) resistivity as a function of the back-gate voltage, measured at room temperature (black line) and $T = 2.7$ K (blue line), using the upper device in panel b. Top inset: Log–Log plot of the conductivity as a function of the carrier density (from data in the main panel). The semi-transparent lines show the standard procedure for the extraction of n^* . Bottom inset: mobility as a function of the gate voltage, calculated according to the Drude model. Black (blue) lines correspond to data at $T = 300$ K (2.7 K); continuous (dotted) lines are data from the upper (lower) Hall bar in panel b. e) first derivative of the Hall conductivity, measured as a function of the back-gate voltage and magnetic field (up to $B = 8$ T, at $T = 0.35$ K). f) longitudinal (black) and Hall (red) conductivity as a function of the filling factor, measured at $B = 2$ T and $B = 8$ T, in the left and right sub-panels, respectively.

for the community to achieve the graphene quality requirements for several applications.^[1]

2.3. Dry Van Der Waals Pick-Up for Ultra-High-Quality Devices

The transport properties of graphene devices (regardless of the “origin” of the material) critically depend on the extrinsic disorder, chiefly resulting from their supporting substrate and/or processing-related contamination.^[93] Dry van der Waals (vdW) encapsulation in hBN flakes is known to successfully mitigate these issues^[19] also when applied to transferred CVD-grown single- and bilayer graphene.^[22,23] Importantly, the strong vdW adhesion between graphene and hBN can be leveraged to directly pick up CVD graphene from conventional Cu foils, pro-

vided that Cu_xO is formed at the graphene/Cu interface.^[20,21] Recently, this technique has been extended to graphene on Cu thin films, both in the form of “ultrafoils”^[94] and epitaxially grown on sapphire.^[42] However, to the best of our knowledge, there is no report on the dry pick-up of graphene from Cu(111) interface.^[41–44] We fully decouple CVD graphene single crystals from the Cu film via post-growth oxidation treatment in an environmental chamber (ambient pressure, humidity 95%, temperature 90 $^\circ\text{C}$, 24 h); the effective oxidation of the interface is supported by optical microscopy images shown in Figure S13 (Supporting Information) as well as Raman analysis (Figure S14, Supporting Information). The oxidation is followed by hBN-mediated vdW pick-up, as sketched in Figure 4a, step (i). Such post-growth oxidation was also performed on samples annealed in H-rich atmosphere, but this process yielded a much lower level of

surface oxide (as confirmed by Raman spectroscopy, Figure S14, Supporting Information), and the strong coupling of graphene to the growth substrate prevented the vdW pick-up. Standard fabrication techniques are then used to process edge-contacted back-gated devices^[19] (Figure 4a, step (ii)), as the two Hall bars shown in Figure 4b. Figure 4c shows a representative Raman spectrum, displaying the typical features of hBN-encapsulated graphene (such as A(2D)/A(G) ≈ 16 and FWHM(2D) ≈ 17 cm⁻¹), consistent with our previous findings on electrochemical transfer from Cu foil followed by encapsulation.^[22] When collecting data over a device-compatible 8×12 μm^2 area, we obtain a statistical distribution of FWHM(2D) peaked at 17 cm⁻¹ (Figure 4c inset), with $\approx 75\%$ of spectra having FWHM(2D) < 20 cm⁻¹, indicating minimal strain fluctuations^[89] and thus suggesting ultra-high carrier mobility.^[87] In Figure 4d we show the longitudinal resistivity ρ of the upper Hall bar, as a function of V_{bg} (applied via the underlying SiO₂/Si substrate). At $T = 300$ K (black curve), we measure a ≈ 1 k Ω peak at charge neutrality, as typically observed in high-quality encapsulated single-layer graphene at room T ,^[95] located at $V_{\text{bg}} = 0.4$ V, indicative of minimal residual doping. The width of this peak quantified as the standard parameter n^* ,^[87] is $\approx 5 \times 10^{10}$ cm⁻² (see Figure 4d, top inset), comparable to the intrinsic thermal broadening.^[95] At $T = 2.7$ K (blue curve), the resistivity peak becomes extremely sharp ($n^* < 10^{10}$ cm⁻²), analogous to Si-gated encapsulated devices based on exfoliated graphene,^[93] while ρ as low as ≈ 30 Ω is measured at high doping levels. In Figure 4d, bottom inset, we convert the resistivity data from the two Hall bars into the carrier mobility μ , again calculated according to the Drude formula. The two devices consistently show comparable performance. At low carrier concentration, μ exceeds 10^5 cm² V⁻¹ s⁻¹ at room T (black curves), setting (to the best of our knowledge) a new standard for graphene grown on Cu thin films.^[42] At $T = 2.7$ K (blue curves), μ as high as 4×10^5 cm² V⁻¹ s⁻¹ is measured, again rivaling exfoliation-based devices.^[93] Figure 4e shows a so-called Landau fan, measured on the upper Hall bar at $T = 0.35$ K. The dark blue areas ($d\sigma_{xy}/dV_{\text{bg}} \approx 0$) correspond to QH plateaus, separated by compressible regions (light blue to red) following linear gate-field trajectories. On top of the standard semi-integer sequence of single-layer graphene ($\nu = \pm 2, \pm 6, \pm 10, \dots$), we observe the lifting of the spin and valley degeneracies promoted by electronic correlation in moderate magnetic fields.^[96] As shown in Figure 4f, left, a QH state at $\nu = 0$ is already defined at $B = 2$ T. This state is of particular relevance for the possible development of topological quantum hardware based on Majorana fermions^[15] upon coupling to superconductors. The observed low-field onset of quantization at $\nu = 0$, apart from further certifying the low-disorder level of the device (see also the Shubnikov-de Haas analysis presented in Figure S15, Supporting Information), represents a key element to facilitate superconducting proximity experiments.^[17] Complete lifting of the four-fold degeneracy within the $N = 0$ Landau level at $B = 8$ T is shown in Figure 4f, right (analogous phenomenology is detected also for higher-index levels).

3. Conclusion

In conclusion, we introduced the growth of high-quality decoupled graphene on Cu films on sapphire using LPCVD condition and non-reducing annealing. The sublimation of the Cu

film, which is a common problem in a LPCVD condition, is suppressed using confinement of the copper film with a sapphire enclosure, which also acts as a source of oxygen during the growth process. Microscopic characterization shows that graphene grows on flat surfaces and does not present ripples. The Cu/graphene interface properties are investigated via LEED, XPS, HR STEM, and ARPES which indicate the presence of a well-ordered thin layer of Cu₂O below graphene. This finding is of extreme importance as it opens novel high-quality graphene growth scenarios not considered until now. Indeed, obtaining graphene on a well-ordered thin layer of Cu₂O(111) holds enticing prospects for both fundamental studies and technological applications. Being one of the first known semiconductors, the first one where excitons were observed,^[97,98] featuring a bandgap exceeding 2.1 eV, with great photocatalytic activity,^[66–68] with facile and non-toxic fabrication routes, Cu₂O(111) might be tested as a promising graphene platform for a variety of novel applications ranging from optoelectronics and sensing to energy conversion and production. Also, the graphene/Cu₂O(111) system might become an active playground to investigate a variety of phenomena such as the spin Hall effect,^[99] novel exciton physics,^[100] anisotropic carrier transport.^[101] Furthermore, the reduced coupling between graphene and the underlying substrates facilitates graphene transfer and allows to obtain high-quality material with state-of-the-art performance. Upon transfer on SiO₂/Si, transport measurements demonstrate excellent performance, with room-temperature mobility exceeding 10^4 cm² V⁻¹ s⁻¹. Full decoupling of the grown graphene is straightforwardly obtained with a post-growth oxidation treatment in an environmental chamber which facilitates dry pick-up of graphene crystals and assembly of high-quality hBN/graphene heterostructures, ultimately yielding carrier mobility $> 10^5$ cm² V⁻¹ s⁻¹. During the production stage of this article, we became aware of a very recent work reporting similar carrier mobility ($\approx 1.25 \times 10^5$ cm² V⁻¹ s⁻¹ at room temperature) in dry picked-up graphene from Cu films on sapphire that, although synthesized in a different way, further shows the potential of this layout.^[102] By synthesizing decoupled, easy-to-transfer graphene directly on a rigid template featuring electronic performance comparable to those of exfoliated flakes, the presented growth approach opens realistic pathways for high-end applications, including the exploration of innovative quantum platforms.

4. Experimental Section

Cu Film Deposition: The Cu film was deposited on single-side-polished single-crystalline 2" *c*-plane sapphire (i.e., α -Al₂O₃(0001)) wafers purchased from Roditi and Silian. The wafers were cleaned by sonication in acetone and isopropanol and then with "piranha" solution (i.e., H₂SO₄:H₂O₂ 3:1) for 15 min, followed by rinsing with DI water. A Cu film with a nominal thickness of ≈ 3 μm was deposited using a thermal evaporator (Moorfield Nano PVD-T15A) at a deposition rate ≈ 0.1 nm s⁻¹ and pressure $\approx 1.6 \times 10^{-5}$ mbar.

Graphene Growth: The sapphire/Cu wafer was diced in samples of 2×2 cm² size where graphene growth was performed. Each die was placed above a *c*-plane sapphire support at a distance of 0.4 mm with the Cu film facing downwards. Four pieces of sapphire were used as pillars to separate the Cu film from the support sapphire (Figure 1a). Pre-annealing of the Cu film and graphene growth was carried out in situ using a commercially available cold-wall reactor (Aixtron BM Pro 4") with

base pressure of 25 mbar. Before graphene growth, the Cu film was annealed at a nominal susceptor temperature of 1040 °C for 10 min in Ar flow (1000 sccm). The surface temperature of the suspended Cu/sapphire was estimated to be ≈ 1000 °C (please see Supporting Information for more details). For the hydrogen annealing experiments, a 5:1 Ar:H₂ (500:100 sccm) flow was adopted at the same base pressure. Graphene growth was performed at the same temperature. Isolated graphene crystals were grown in 15 min under Ar:H₂:CH₄ (900:50:1 sccm) flow, while continuous graphene films were obtained with a CH₄ flux of 2 sccm (same Ar and H₂ fluxes) and by prolonging the growth time to 25 min. When increasing the CH₄ flux, emergence of spurious (i.e., non-aligned) crystallographic orientations was noticed. Finally, the reactor was cooled under the flux of Ar (1000 sccm) to below 50 °C before venting. At this temperature the oxidation of Cu in air was negligible.^[103]

Electrochemical Transfer: Graphene was transferred from Cu film to 285 nm layer of SiO₂/Si using electrochemical transfer. Initially, CVD grown graphene on Cu film was coated with a 100 nm poly(methyl methacrylate) (PMMA) layer and baked at 90 °C for 2 min. Then, a 1.5- μ m Polypropylene carbonate (PPC) layer was spin-coated and baked for 2 min. A Polydimethylsiloxane (PDMS) frame was attached to the edge of the sample to use as a support during the whole transfer process. Graphene was electrochemically delaminated from Cu^[104,105] in 1 M NaOH with applied voltage of -2.5 V. A strip of Cu foil using a conductive silver paste was attached to make electrical contact to the Cu thin film (Figure 3a). During spin coating of polymers, a small portion at the edge of the Cu film was masked using adhesive tape to provide an open area for silver paste contact. Another strip of Cu foil was used as a counter electrode. After delamination, the graphene/polymer stack was cleaned by floating it two times on the surface of DI water and then dried in air to remove any residual water. As described previously,^[71,73] a custom-built setup was used, to align and laminate the dry graphene/polymer stack to the target Si/SiO₂ wafer placed on heating stage, then the temperature was raised to 85 °C and kept for 5 min to ensure strong adhesion of graphene on SiO₂/Si substrate. The PDMS frame was detached from the sample with tweezers and the PPC and PMMA were removed by immersing in acetone for over 3 h, followed by isopropanol rinsing. The graphene on SiO₂/Si was immersed in remover (AR600-71) to further clean the remaining polymer residues, as reported in our previous work.^[72]

Dry Transfer and Encapsulation: To prepare the sample for dry pick-up transfer, the Cu film at the Graphene-Cu interface was oxidized using environmental chamber oxidation (ambient pressure, humidity 90%, temperature 80 °C, 24 h). hBN flakes were mechanically exfoliated onto SiO₂/Si^[106] and suitable candidates (≈ 30 nm thickness, ≈ 50 μ m lateral dimension, crack and wrinkle-free) were selected via optical microscopy and/or atomic force microscopy. A polymeric stamp, composed of a poly(bisphenol A carbonate) (PC) film was then employed on a few-mm thick polydimethylsiloxane (PDMS) block, to isolate an hBN flake.^[107] The flake was aligned over a graphene crystal on Cu₂O/Cu/sapphire using a home-built setup^[73] and smoothly brought in contact exploiting the thermal expansion of the PDMS block (typically ramping the setup temperature from 40 °C to 80 °C). The stamp was then retracted by cooling with natural air convection, leading to complete pick-up of the graphene area covered by hBN (at the moment of writing this manuscript, the process has been consistently reproduced > 10 times; exposed graphene areas were often detached by PC alone, however with reduced reproducibility and control). The graphene encapsulation was concluded by picking up a second hBN flake, and the heterostructure was finally released onto SiO₂/Si at 180 °C, following Ref. [107]. The resulting heterostructure was characterized using scanning micro-Raman spectroscopy to select target areas for subsequent device fabrication.

Characterization: An optical microscope (Zeiss Axioscope 7 equipped with AxioCam 208 color camera) was used to perform optical imaging of the samples. Atomic force microscopy (AFM) characterization was carried out with Bruker Dimension Icon microscope and Raman characterization was carried out with a Renishaw InVia spectrometer. Raman spectroscopy of as-grown graphene on Cu/sapphire was performed using a 473 nm laser, ≈ 2.5 mW power, and 5 s exposure. For graphene transferred on Si/SiO₂, a 532 nm laser was used, with ≈ 1 mW power and 1 s exposure.

LEED measurements were carried out using Er-LEED 150 from Specs, with the sample at room temperature, mounted on a 4-axes motorized manipulator from VG.

ARPES and XPS measurements were carried out in a Specs Flex system, at room temperature. The samples were mounted on a 5-axe manipulator and positioned in front of the objective lens of a Specs Astraio 190 electron analyzer. The UV light source was a Specs micro-Sirius, using Helium gas plasma, while the X-ray source was a Specs XR-50, with the Al anode selected, emitting at the K α line at 1486.61 eV.

The preparative for HR STEM study and the measurements were performed as follows. A cross-sectional specimen with a final thickness of 50 nm was prepared by FIB milling using a Helios Nanolab FIB/SEM (Thermo Fisher Scientific). A thin layer of platinum (200 nm) was deposited over the target area using the electron beam (2 nA, 5 kV) prior to ion-beam exposure. A standard in situ procedure was adopted for lift-out. A final polishing step was carried out at a voltage of 2 kV to reduce the FIB-damaged layer on the surface. HR STEM images were acquired on a probe-corrected ThermoFisher Spectra 30–300 S/TEM operated at 300 kV, using a High-Angle Annular Dark Field (HAADF) detector with a beam current of 50 pA. The convergence angle was set to 25 mrad, corresponding to a sub-angstrom electron beam. Compositional maps were acquired using Velox, with a probe current of ≈ 150 pA and rapid rastered scanning Energy-Dispersive X-Ray (EDX) on a Dual-X setup comprising two detectors on either side of the sample, for a total acquisition solid angle of 1.76 Sr.

Device Fabrication and Electrical Transport Measurements: Hall bar devices were fabricated using a standard electron beam lithography fabrication process. First graphene channels were patterned using a PMMA etch mask (AR-P-672.045) followed by etching the exposed region using Reactive Ion Etching (RIE) system (Sistec) at (45 W (CF₄/O₂ 20/2 sccm for encapsulated graphene) and (35 W with Ar/O₂ flow of 5/80 sccm for graphene on SiO₂). The second lithography step was used to define the metal contacts followed by metallization (Cr/Au, 5/50 nm) using an electron beam evaporator. Top contacts were used for graphene on SiO₂, and edge contacts for hBN-encapsulated graphene. For graphene on SiO₂, electrical transport measurements were performed in ambient conditions using a custom-made probe station with tungsten tips on micro positioners. Electric field effect was measured using a pair of Keithley 2450 source-measure units, for a 4-terminal resistance measurement and back-gate sweep. For hBN-encapsulated graphene, we performed 4-probe measurements with low-frequency (≈ 13 Hz) lock-in detection, either in a constant current (≈ 100 nA), or constant voltage configuration (0.1 mV). The zero-field measurements (Figure 4d) were performed in a “ICE 3K INV” cryostat, the magnetotransport measurements (Figure 4e,f) in a “ICE 300 mK He-3 Continuous” cryostat equipped with an 8 T superconducting coil.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

chemical vapor deposition, copper film, Cu₂O, dry pick-up, graphene, high-mobility

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