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Supercurrent time division multiplexing with solid-state integrated hybrid superconducting electronics

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Time-division multiplexing of cryogenic signals is a promising approach to reduce space requirements, shorten cooldown times, and increase the number of quantum devices measured per cooldown. We demonstrate time-division multiplexing of non-dissipative supercurrents using voltage-controlled hybrid superconducting demultiplexers. These chips integrate superconducting Josephson Field Effect Transistors including Al superconducting electrodes, proximitized semiconducting InAs channels, and hafnium oxide gate insulators. Each transistor fully suppresses the switching current and increases the resistance 20 times under a gate voltage of −4.5 V. A demultiplexer with one input and eight outputs showed a non-dissipative input range of ±2 μA, operating up to 100 MHz in signal frequency, and 100 kHz in switching frequency at 50 mK. It achieved near-zero insertion loss in the superconducting state and an $\frac{ON}{OFF}$ ratio of 17.5 dB. By optimizing the signal layout, the operation was extended up to 4 GHz using a demultiplexer with two outputs.

In the past decades, there has been tremendous progress in the theoretical and experimental development of a wide range of quantum devices operating at cryogenic temperatures, where phase transitions, reduced thermal noise, and minimized interactions with the surrounding environment can be achieved. Superconducting[1–3] and spin qubits[2,4,5], parametric amplifiers[6–9], diodes[10–12], and single photon detectors[13–15], are only a few examples of the devices proposed and manufactured. Along the same side, cryogenic temperatures are mandatory to study hot topics in quantum physics, such as spin-dependent supercurrent[16], topological phase transitions[17–19], superconductivity-quantum Hall effect interaction[20–22], and many-body electron systems[23–25].

In a conventional cryostat, N signal lines come from (to) room temperature electronics and travel to (from) the low-temperature plates connecting to the N ports of the quantum device under test (QDUT) (Fig. 1a). Each signal line significantly impacts the cryostat's costs, space occupied, and temperature stability. Thus, the number of cables is a significant constraint in testing and using of very-large-scale-integrated (VLSI) quantum devices. For instance, one of the most advanced quantum machines, the quantum computer Google Sycamore, uses more than 200 RF coaxial cables to control only 54 qubits[26,27]. To reduce the required space, minimize the cooldown time, and increase the number of measurable devices per cooldown, time division multiplexing (TDM) of signal lines is needed to route signals to the QDUT. In a TDM-cryostat, only one signal line reaches the lowest temperature plate to connect 2^N ports of the QDUT using N control lines (Fig. 1b).

Nowadays, electromechanical switches are usually involved in TDM of signals at cryogenic temperatures down to a few mK, with the drawbacks of a large amount of volume occupied ($\sim 100\,cm^3$), reduced I/O lines, and a high switching time (~10 ms)[28–30]. Complementary Metal Oxide Semiconductor solid-state solutions operating at cryogenic temperature, i.e., cryo-CMOS, offer the advantage of a reduced volume together with an increased number of I/O lines and faster-switching events (~1 ns), allowing at the same time to achieve line-to-line isolations of 30 ÷ 40 dBs[31–34]. On the other hand,

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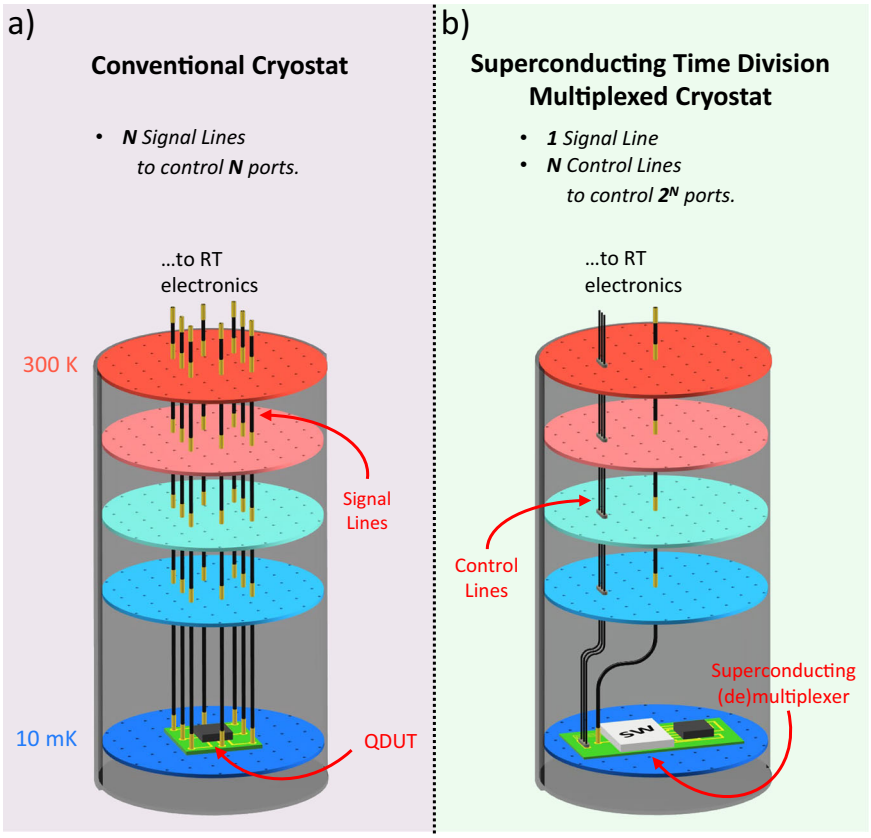


Fig. 1 | Comparison between conventional and superconducting TDM cryostats. a A conventional cryostat needs N signal lines to control N ports of the QDUT. **b**) A superconducting TDM-cryostat features N control lines and one signal line to control 2^N ports of the QDUT. The schematic representations are intended to represent the input or the output lines of the QDUT.

static power dissipation accounts for the increase of the temperature of the cold plate of tens of mKs[31,33], while an insertion loss of 1 ÷ 3 dBs is usual in the ON-state due to the Ohmic behavior of the chip[33,34]. In quantum computing, it is noteworthy that the deployment of TDM using cryo-CMOS platforms remains incompatible with scalable, high-fidelity control of superconducting transmon qubits. This incompatibility arises from significant thermal radiation emitted by the multiplexer, necessitating the thermalization of signals between the demultiplexer's output and the quantum chip via a well-thermalized attenuator[33,34]. Along with the previous solutions, more exotic TDM demonstrations are proposed using platforms based on SiGe-2DEG[35], GaAs-HEMTs[36,37], and InAsNWs[38]. In this context, TDM with a superconducting solid-state multiplexer promises short downtimes between control switching events, near-to-0W static power dissipation, negligible heat injection, and a minimized insertion loss. In recent years, few demonstrations of proof-of-concept superconducting switches have been documented[39–41]. On the other hand, considerable insertion loss and static power required in the ON-state[39], reduced operating band[40,41], and a limited number of output ports (2 at maximum)[39–41], are the major drawbacks highlighted.

Hybrid superconductor-semiconductor architectures enable ideal platforms to develop Josephson Field Effect Transistors (JoFETs) for supercurrent multiplexing[42–46]. The hybrid super-semi JoFET is the key to implementing a two-state ON/OFF superconducting/resistive building block[47]. The gate tunability of the critical current, as well as the gate tunability of the normal-state resistance, are the fundamental aspects involved in the supercurrent multiplexing operation. In the III-V compound group, InAs is the most common semiconductor employed in the manufacturing of JoFETs, thanks to the optimal superconducting proximity effect[42–44,48–51], which provides the electron gas hosted by the InAs layer the ability to support a supercurrent. Among InAs-based platforms, we recently proposed InAs on Insulator (InAsOI) as a new convenient platform to develop planar hybrid superconducting electronics[52–54]. Unlike other InAs architectures, the InAsOI features an InAs epilayer grown onto a cryogenic electrical insulating InAlAs metamorphic buffer. The InAsOI allows the electrical decoupling of surface-exposed adjacent devices together with the capability of achieving the superconducting proximity effect with high critical current density integration. Irrespective of the fabrication methodology customary to GaAs-based heterostructures, the InAsOI epitomizes the counterpart of the silicon-on-insulator (SOI) architecture apt for superconducting technologies, wherein proximitized InAs and the cryogenic electrical insulating InAlAs substitute silicon and silicon oxide layers of SOI, respectively.

Here, we report on the TDM of non-dissipative supercurrents with voltage-actuated hybrid superconducting demultiplexers able to reduce the number of signal lines of a conventional cryostat. As ON/OFF building blocks, we developed InAsOI-based JoFETs featuring Al as superconductor and HfO_2 as gate insulator, able to suppress the switching current entirely and to increase the normal-state resistance by 20 times with a gate voltage of −4.5 V. We proposed a superconducting demultiplexer with 1 input and 8 outputs operating at 50 mK up to 100 MHz in signal frequency and 100 kHz in switching frequency, featuring an insertion loss of ~ 0 dB in the superconducting state, and an $\frac{ON}{OFF}$ ratio of ~17.5 dB. The operational range of signal frequency was effectively broadened by designing a superconducting demultiplexer with a single input and dual outputs, incorporating an optimized microwave signal transport layout that concurrently mitigates the influence of parasitic electrical elements.

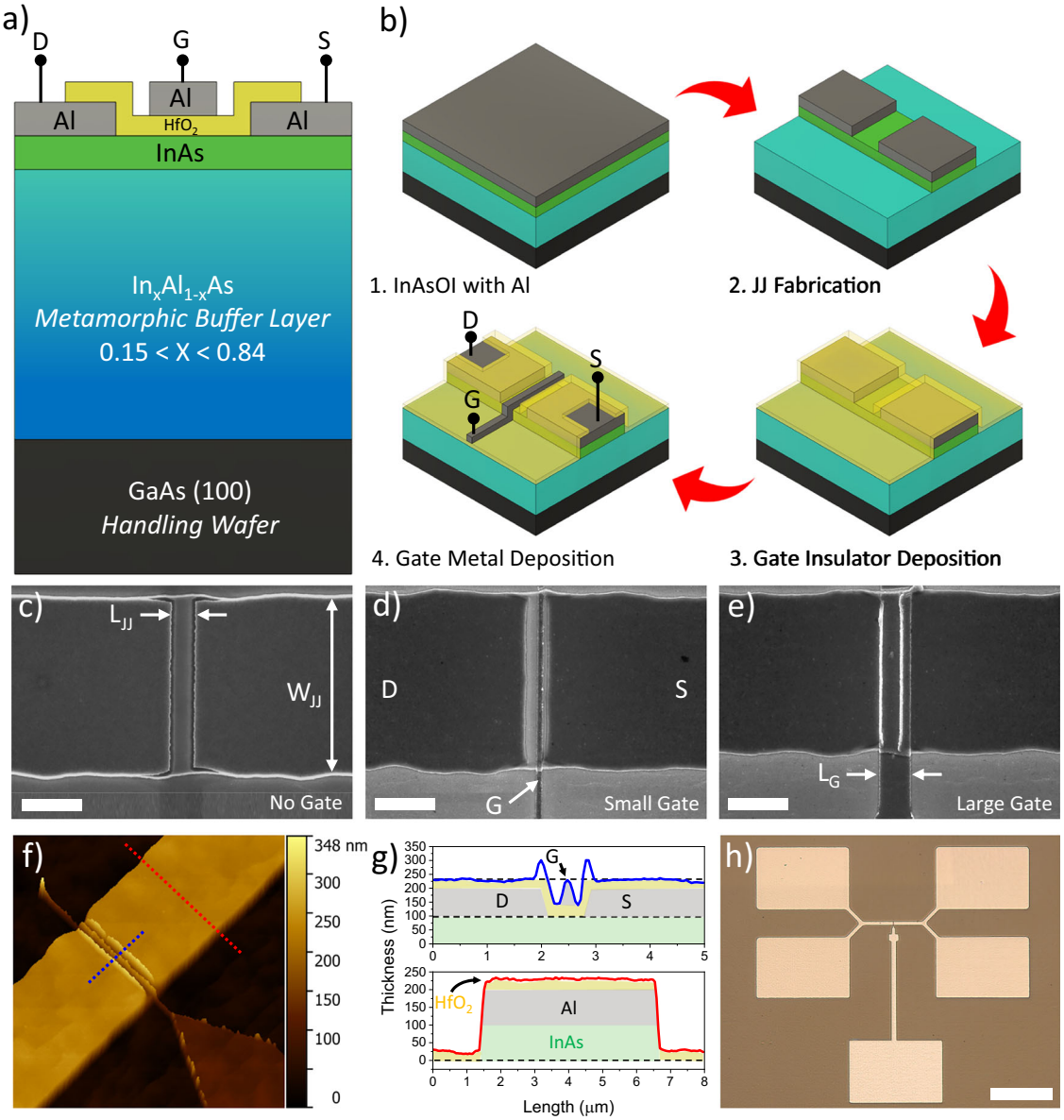


Fig. 2 | Josephson Field Effect Transistors with InAsOI: concept, manufacturing process, and morphologic characterization. a Cross-section structure of a JoFET with InAsOI. **b** Fabrication process of a JoFET with InAsOI: 1. Superconductive Al deposition onto InAsOI; 2. JJ fabrication via MESA and Al wet etching; 3. Gate insulator deposition via ALD; 4. Gate metal deposition. **c**–**e** Top-view SEM images (10k ×) of JoFETs with W_{JJ} = 6 μm and L_{JJ} = 800 nm before gate fabrication (**c**), and after small (L_G = 200 nm) (**d**) and large (L_G = 1000 nm) (**d**) gate manufacturing; the scalebar is 2 μm. **f** xy-plane tilted AFM z-profile of a JoFET featuring W_{JJ} = 6 μm, L_{JJ} = 1200 nm, and L_G = 100 nm. **g** AFM thickness profiles extrapolated from the red and blue dashed line in (**f**). **h** Optical microscope image of the 4-terminal JoFET architecture. The scalebar is 100 μm.

The constructed device underwent validation at frequencies reaching up to 4 GHz at 50 mK, demonstrating an insertion loss of approximately 0 dB within the superconducting state and exhibiting an $\frac{ON}{OFF}$ ratio of ~16 dB. The reciprocity of the circuits allows, in principle, reversed operations of the proposed devices as a multiplexer by inverting the I/O ports.

Results and discussion

InAsOI-based Josephson Field Effect Transistor fabrication

The cross-section of a Josephson Field Effect Transistor fabricated on the InAsOI platform is shown in Fig. 2a.

The JoFET is built upon a Molecular Beam Epitaxy (MBE)-grown InAsOI stack consisting, from bottom to top, of a 500-μm-thick semi-insulating GaAs (100) substrate, a ~1.5-μm-thick step-graded $In_xAl_{1-x}As$ metamorphic buffer with X increasing from 0.15 to 0.84, and a 100-nm-thick InAs semiconductive epilayer[52]. The InAs layer is *n*-type doped (extrinsically undoped) due to the InAs natural surface electron accumulation layer[55,56] and deep energy donor levels in the InAlAs band gap[57]. For the InAs epilayer, a sheet electron density (n_{2D}) of 1.35 × 10^{12} cm^{-2} and a mobility (μ_n) of 6.7 × 10^3 cm^2/Vs were measured at 3 K from Hall measurements. The InAlAs metamorphic buffer behaves as an electrical insulator at cryogenic temperatures[52]. Figure 2b depicts the fabrication process of the JoFET. A 100-nm-thick Al layer was deposited onto InAsOI, which acts as the superconductor of the JoFET (Fig. 2b.1). JoFETs were fabricated via aligned lithographic steps. First, Al and InAs MESA were defined by UV-lithography and manufactured by successive Al and InAs wet etching, setting the Josephson Junction (JJ) width (W_{JJ}) and exposing the InAlAs layer. Then, the JJ length (L_{JJ}) was defined by electron-beam-lithography and Al wet-etching, leaving the underneath InAs unaffected (Fig. 2b.2). A ~30-nm-thick HfO_2

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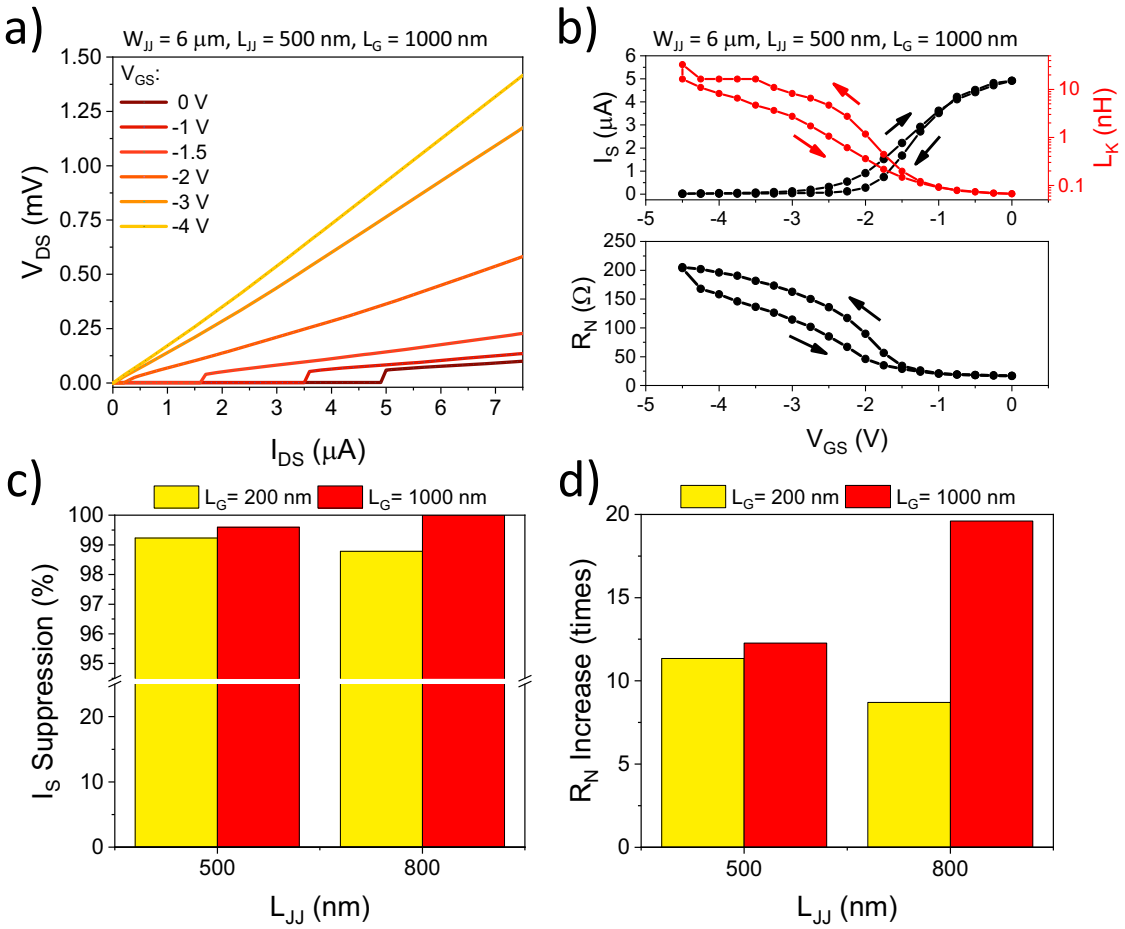


Fig. 3 | InAsOI-based Josephson Field Effect Transistors electrical characterization. a Gate-dependent voltage vs. current characteristics of a JoFET featuring $W_{JJ} = 6\,\mu m$, $L_{JJ} = 500\,nm$, and $L_G = 1000\,nm$. **b** Upward and downward gate-dependent switching current, Josephson inductance, and normal-state resistance of a JoFET featuring $W_{JJ} = 6\,\mu m$, $L_{JJ} = 500\,nm$, and $L_G = 1000\,nm$. **c**, **d** Switching current suppression (**c**) and normal-state resistance increase (**d**) of JoFETs featuring different L_{JJ} and L_G values.

dielectric layer was conformably deposited via Atomic Layer Deposition (ALD) and used as the gate insulator (Fig. 2b.3)[58]. The ALD was performed at an optimized temperature of 130 °C to preserve the Al/InAs superconducting and transport properties[59]. Eventually, the metallic gate was fabricated by electron-beam-lithography and tilted Ti/Al deposition (Fig. 2b.4), which allowed to conformably cover acute angles left by the InAs wet etching (Fig. S1). We realized superconductor-semiconductor-superconductor Al-InAs-Al JoFETs with W_{JJ} of 6 µm, L_{JJ} from 500 to 1250 nm, and gate lengths (L_G) from 100 to 1000 nm. Figure 2c–e show Scanning Electron Microscopy (SEM) images of JoFETs before and after gate fabrication, from which one can appreciate that the metallic gate is aligned and deposited in the middle of the JJ with a precision of ±150 nm, regardless of the gate length. SEM analysis of JoFETs with different values of L_{JJ} and L_G is reported in Fig. S2. Figure 2f, g report the thickness profile of the JoFET surface obtained through Atomic Force Microscopy (AFM) analysis. Finally, an optical microscope photograph of the entire device is shown in Fig. 2h, from which the 4-terminals architecture of the JoFET, meant for the electrical characterization, can be appreciated.

InAsOI-based Josephson Field Effect Transistor electrical characterization

JoFETs were measured in a dilution fridge equipped with a z-axis superconducting magnet and a DC measurement setup (Fig. S3); the electrical characterization was performed at 50 mK. Figure 3a shows gate-dependent V-I characteristics of a JoFET featuring $W_{JJ} = 6\,\mu m$, $L_{JJ} = 500\,nm$, and $L_G = 1000\,nm$. The switching current (I_S) was extracted from the V–I curves as the largest current at 0-voltage drop, while the normal state resistance (R_N) is estimated as the V–I curve slope above I_S.

By decreasing the gate voltage, a reduction of I_S and an increase of R_N is observed. This behavior is confirmed for all the JoFETs tested, regardless of their morphological properties (Fig. S4 left column).

Figure 3b shows the I_S and R_N gate dependence extracted from Fig. 3a. The top panel of Fig. 3b also reports the resulting linear-regime Josephson inductance ($L_K = \frac{\hbar}{2e \times I_S}$, where $\hbar$ is the reduced Plank's constant and e is the elementary charge). For all the curves, a sigmoidal behavior was observed with the gate voltage, with an evident hysteresis between the upward and downward scans, presumably related to electrical traps in the insulator or at the InAs/insulator interface[60,61]. In summary, for all the JoFETs fabricated, the higher the V_{GS} value, the higher the switching current (the lower the normal state resistance), and vice versa (Fig. S4 middle column). The zero-voltage and gate-dependent electrical properties of JoFETs rely on the specific transistor morphology. With the increase of L_{JJ}, a reduction of I_S and an increase of R_N is obtained at $V_{GS} = 0$ V, as expected (Fig. S5). Moreover, at $V_{GS} = 0$ V, the larger the gate length, the lower the switching current (the higher the normal state resistance), regardless of the interelectrode separation (Fig. S5). To quantify the ability of the gate to tune the superconducting and transport properties of the JoFETs, we defined the I_S suppression factor, namely $I_{Sup} = 1 - \frac{I_{S@V_{GS}=-4.5V}}{I_{S@V_{GS}=0V}}$ (Fig. 3c), and the

R_N increase factor, namely $R_{Inc} = \frac{R_{N@V_{GS}=-4.5V}}{R_{N@V_{GS}=0V}}$ (Fig. 3d). For both the interelectrode separations tested (L_{JJ} = 500 or 800 nm), higher I_{Sup} and R_{Inc} factors were obtained in the case of wider gates compared to the thinner ones, namely L_G = 1000 nm instead of L_G = 200 nm. In addition, longer JJs and more extended gates together gave the best I_{Sup} and R_{Inc}. In the case of the JoFET with L_G = 1000 nm and L_{JJ} = 850 nm, a 100% switching current suppression together with ~20 times increase of the normal state resistance was obtained, changing the gate voltage in the range from 0 to −4.5 V. The higher R_{Inc} factor obtained with wider gates is directly related to a larger part of InAs tuned in electron density with the applied gate electric field. At the same time, the larger gate decreases uniformly the Fermi velocity in the semiconductor channel, resulting in a larger effective barrier between the semiconductor and the superconductor. This leads to a less efficient Andreev conversion at the super/semi interface with a stronger suppression of the supercurrent compared to the narrower gate configuration. Remarkably, a negligible leakage current was collected in the gate voltage operation range (Fig. S4 right column). Additional information about the temperature and magnetic field-dependent electrical behavior of the fabricate JoFETs can be found here[54]. I_{Sup} and R_{Inc} achieved for InAsOI-based JoFETs are on par with the top values obtained in other gate-tunable-critical-current platforms, such as those based on InAs[42,59,62] and Ge[45,63,64] quantum wells (QWs), InAs[44] and metallic[65] nanowires (NWs), InAs nanosheets (NSs)[66], and graphene[46,67] (for a comparison see Fig. S6 and Table S1). This makes InAsOI a valuable candidate for implementing cryogenic hybrid superconducting electronics, and the InAsOI-based JoFET a promising circuital element acting as a two-state ON/OFF superconducting/resistive building block.

InAsOI-based superconducting 1-input-8-outputs analog demultiplexer

We now focus on developing a superconducting 1-input-to-8-outputs (1I8O) analog demultiplexer operating at 50 mK. The roles of the I/O ports can be, in principle, reversed to operate the proposed device as a multiplexer. Figure 4a depicts the schematic diagram of the hierarchical architecture of the demultiplexer, where three signal splitting levels are obtained involving 14 JoFETs ($JoFET_0$ to $JoFET_{13}$), one input line (I_0), eight output lines (O_0 to O_7), and six control lines (G_{00} to G_{21}). Two indexes characterize control lines; the first one, ranging from 0 to 2, refers to the three splitting levels (moving from left to right in the scheme of Fig. 4a), the second identifying the bottom (value of 0) or top (value of 1) output branch of each splitting node. Signal and control lines in the schematic representation are highlighted with red and blue colors, respectively, to improve the readability of the diagram.

The superconducting signal can be hierarchically divided from the input to one of the two following outputs, depending on the gate control settings of each signal-splitting node. The number of required JoFETs (U) increases with the number of splitting levels (M) as $U = \sum_{i=1}^{M} 2^i = 2^{M+1} - 2$, while the number of output signals (O) increases with the number of control lines (N) as $O = 2^{\frac{N}{2}}$. Remarkably, the number of outputs can be improved to 2^N by using cold NOT logic gates to invert one of the controls in each signal-splitting level. To effectively accomplish a reduction in control lines, it is imperative that the NOT logic gates, which function at cryogenic temperatures, be situated at the same cold stage as the superconducting demultiplexer.

Figure 4b depicts the schematic representation of the JoFET in the non-gated superconducting state, i.e., the ON state, and in the gated resistive state, i.e., the OFF state. In the ON state (V_{GS} = 0 V), the JoFET acts as an inductor with value L_K; conversely, in the OFF state (V_{GS} = −4.5 V), the JoFET works as a resistor with value R_N. The two capacitors between the gate and drain (C_{GD}) and gate and source (C_{GS}) terminals represent the major parasitic elements for both gate settings. The contribution of the JJ capacitance is considered negligible[68].

In the DC ON state, the current (and the power) through the JoFET totally flows into the inductive branch (Fig. 4b top). This trend is suppressed with the increase of the operating frequency by the gate capacitors, providing a path to the AC-grounded gate terminal. We defined the JoFET ON-state maximum operational frequency ($f_{MAX_{ON}}$) as the frequency at which the power provided by the drain to the source decreases by 10% (−0.46 dB) compared to its DC value. Based on the values reported in Table S2, $f_{MAX_{ON}} = 6GHz$ was retrieved from the simulations. Similarly, in the OFF state, the parasitic gate capacitors limit the maximum operation frequency of the JoFET ($f_{MAX_{OFF}} = 17GHz$) shunting R_N. The overall maximum operating frequency (f_{MAX}) of the JoFET can be expressed as $min(f_{MAX_{ON}}, f_{MAX_{OFF}})$, resulting in $f_{MAX} = f_{MAX_{ON}}$. A detailed discussion is provided in Section 5 of the Supporting Information. f_{MAX} can be increased to higher frequencies by designing JoFETs with a reduced gate capacitance by downsizing the gate capacitor area. Operating JoFETs at higher frequencies also requires considering the wavelength period in GaAs (λ_{GaAs}), namely 25 ÷ 2.5 mm for 1 ÷ 10 GHz frequencies. If λ_{GaAs} is comparable to the dimension of the fabricated chip, a specific layout with electromagnetic wave transport through waveguides is mandatory to achieve negligible insertion loss.

Figure 4c shows a false-color optical microscope image of the 1I8O demultiplexer fabricated on InAsOI. The chip is 5.5 × 3 mm^2 and features two routing levels of 50-µm-width Al superconducting traces: the underneath for the signal lines (red traces) and the overlying for the gate control lines (blue traces). A HfO_2 layer with 30 nm thickness was used as a gate and metal trace insulator. Each signal line is provided with two pads to perform 4-terminal electrical measurements (Fig. S7). JoFETs with W_{JJ} = 4 µm, L_{JJ} = 500 nm, and L_G = 9.5 µm were fabricated as ON/OFF building blocks. Figure 4d shows an overlap between a signal and a gate control line where a JJ is present, i.e., the JoFET. On the other hand, Fig. 4e exhibits an overlap without active elements, which is used to reach positions on the chip with control lines that cannot be reached without two routing levels.

Table S3 reports the 1I8O demultiplexer truth table. For each gate control configuration, only one input-to-output path is fully superconductive, while all the remaining have at least one JoFET in the dissipative state. The signal line resistance is 0 Ω in the case of the non-dissipative path or equal to 1 × R_N, 2 × R_N, or 3 × R_N according to the number of JoFETs in series in the OFF state along the specific input-to-output line. As a case of study, we focused on having the I_0-O_4 line superconductive (Fig. 4f), with gate control lines set to $V_{G00} = V_{G11} = V_{G21} = 0V$ and $V_{G01} = V_{G10} = V_{G20} = -4.5V$. Figure S8 depicts the schematic lumped element diagram of the demultiplexer with the applied gate settings to clarify the electrical configuration obtained. Figure 4g shows V-I characteristics of all the signal lines. As desired, only I_0-O_4 exhibits a 0 Ω resistance path up to the switching current, while all the other lines present a dissipative path. The non-dissipative dynamic input range of the superconducting demultiplexer consequently goes from -I_S to I_S. Line resistances (R_{Line}) are summarized in Fig. 4h, from which we can observe that the $R_{Line}/R_{N@V_{GS}=-4.5V}$ ratio agrees with what is expected (Table S3). By changing the gate control lines setting, the non-dissipative path can be transferred to one of the other signal lines, as reported in Fig. S9 where I_0-O_6 was selected as fully superconductive. This result stem from the good reproducibility of the electrical properties of both JoFETs and signal lines (Fig. S10). Over the 14 JoFETs integrated, a switching current of 1.98 ± 0.52 µA (average ± standard deviation) is calculated, leading to a percentage coefficient of variation (CV) of 26.2 % (Fig. S10a). Only the $JoFET_7$ exhibited a switching current strongly far from the average; by removing this contribution, a switching current of 2.09 ± 0.31 µA (CV = 14.8%) is obtained. Differently, the signal line resistance for input currents higher than the switching current, which is related to the

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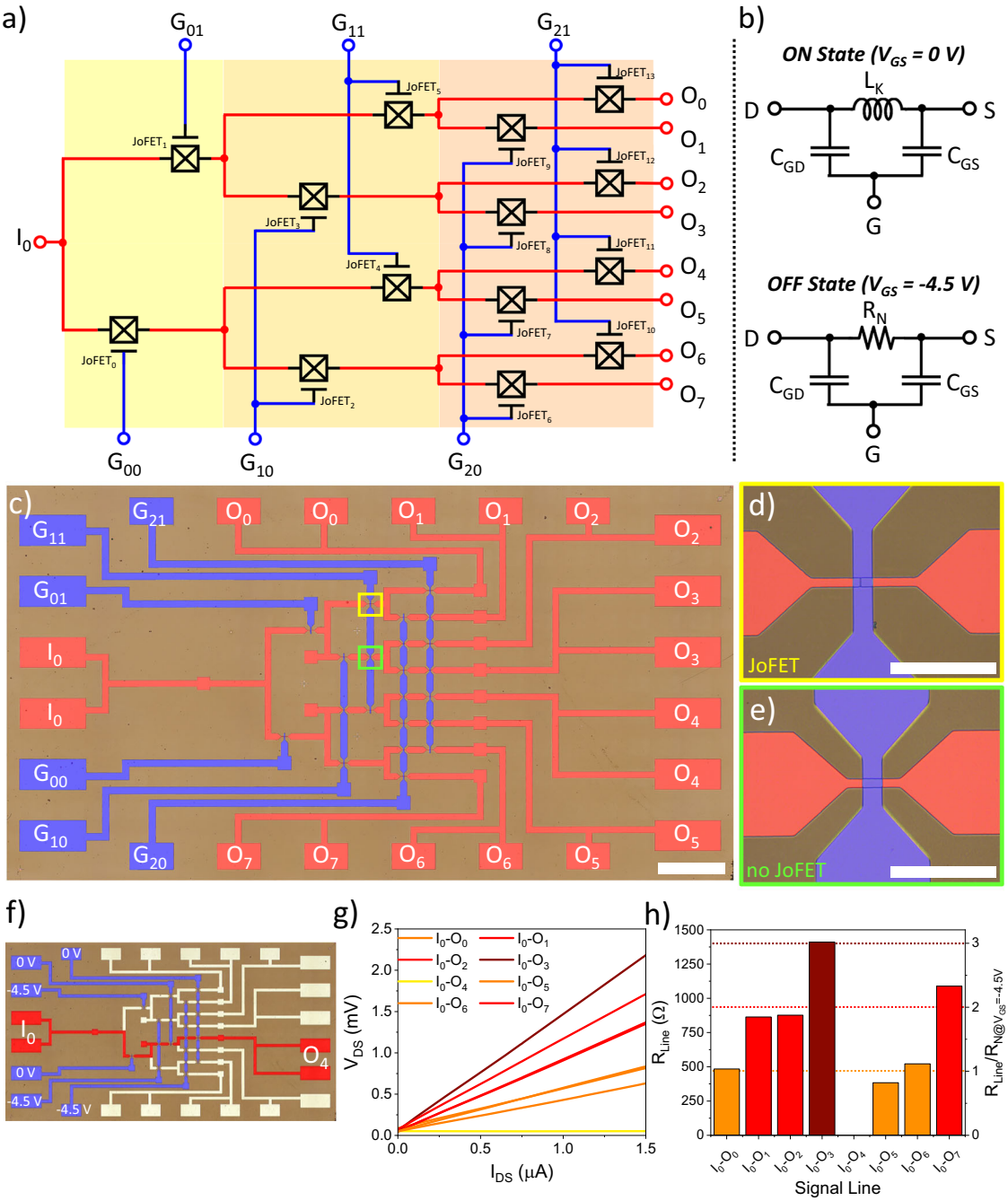


Fig. 4 | Concept, morphological, and DC electrical characterization of the superconducting 1-input-8-outputs analog demultiplexer. a Schematic diagram of the superconducting 1I8O demultiplexer. **b** Electrical lumped model of the InAsOI-based JoFET. **c** False-color optical microscope image of superconducting 1I8O demultiplexer; the scalebar is 500 μm. **d**, **e** False-colors optical microscope image of an overlap between a signal and a gate control line with (**d**) or without (**e**) a JoFET; the scalebar is 50 μm. **f** False-color optical microscope image of the superconducting 1I8O demultiplexer, highlighting the chosen superconducting path and the gate control configuration. **g** V-I characteristics of all the 1I8O demultiplexer signal lines with the gate configuration shown in (**f**). **h** Line resistances (left) and normalized line resistances (right) of all the 1I8O demultiplexer signal lines with the gate configuration shown in (**f**).

reliability of the transport properties of the JoFETs, was calculated as 84.2 ± 3.4 Ω (CV = 4.0 %) (Fig. S10b). The achieved results indicate that by introducing VLSI technological steps, a superconducting demultiplexer with a higher number of reliable output lines can be fabricated.

We then evaluated the time-resolved electrical behavior of the superconducting 1I8O demultiplexer. We simultaneously measured signal lines I_0-O_4 and I_0-O_6 while switching between two gating configurations to have only one line at a time in the non-dissipative state. The gate voltages were switched at a switching frequency (f_{SW}) of 100 Hz from $V_{G10} = -4.5V$ and $V_{G11} = 0V$ to cancel the resistance of line I_0-O_4, to $V_{G10} = 0V$ and $V_{G11} = -4.5V$, to make the path I_0-O_6 superconductive, while leaving all the other gate control lines to $V_{G00} = V_{G21} = 0V$ and $V_{G01} = V_{G20} = -4.5V$ (see Table S3 and Fig. 5a top). The electrical characterization was performed in a dilution fridge equipped with a very-large-frequency (VLF) measurement setup (cut-off frequency ~ 45 kHz) with load resistances (R_L) of ~200 Ω due to the cryostat wire impedance (Fig. S11). The signal-line input current (I_{IN}) is ~1.3 μA. The central panel of Fig. 5a shows signal line voltages: only one line per time exhibits a zero voltage drop corresponding to the line with all the JoFETs in the ON state. Voltage drops measured for both

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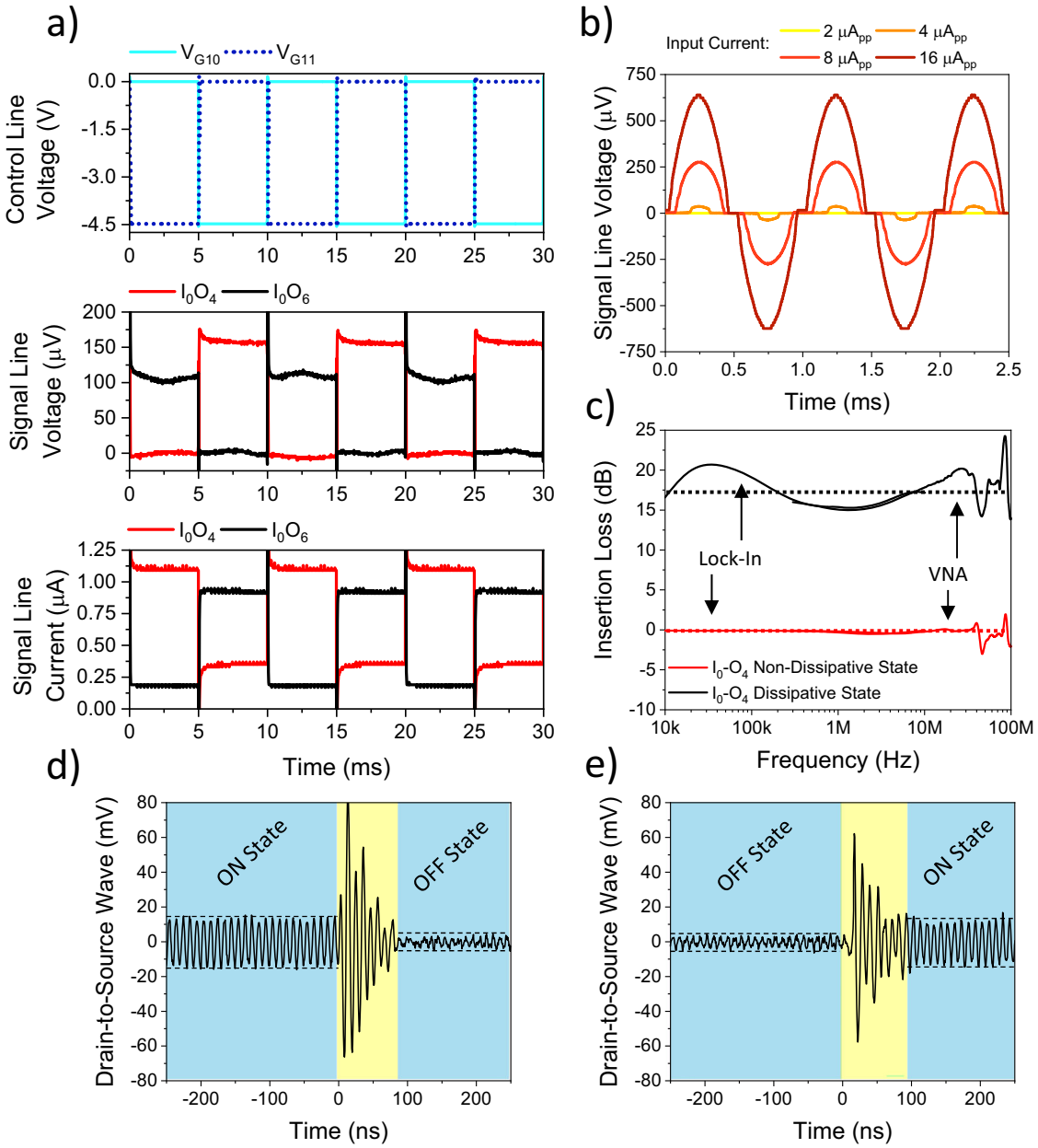


Fig. 5 | Time-resolved and AC electrical characterization of the superconducting 1-input-8-outputs analog demultiplexer. a Time-resolved electrical behavior of the superconducting demultiplexer. Time-dependent control line voltages (top), signal line voltages (middle), and signal line currents (bottom). **b** Time-resolved I_0-O_4 signal line voltage with different peak-to-peak input currents. **c** Frequency-resolved insertion loss of signal line I_0-O_4 in the non-dissipative and dissipative states. Measurements are taken with a lock-in amplifier and a VNA for low and high-frequency ranges, respectively. **d**, **e** Drain-to-source wave voltage (f = 100 MHz) measured during the turn-OFF (**d**) and turn-ON (**e**). The blue areas indicate the steady state behavior, while the yellow area indicates the transient.

the lines in the dissipative state are not identical due to the small differences in the gated line resistances (Fig. 4h and S10c). Correspondingly, the input current is divided into the two signal lines in agreement with the total line resistance (see Fig. 5a, bottom). Specifically, the signal line current does not reach 0 A when the line is in the dissipative state due to the cryostat wiring impedance in series to the switch (R_L ~ 200 Ω). This is a remarkable point to consider when selecting the impedance loads that the superconducting switch can drive. We defined the rise (t_r) and fall (t_f) time as the time the signal line voltage takes to go from 10% to 90% of its peak value, and vice versa, for the rise and fall time, respectively. We evaluated t_r=t_f ~ 50–75 μs. Since for a square signal, the contribution of the frequency harmonics higher than the carrier frequency is relevant only in the transition between the peak-to-peak value, the maximum switching frequency ($f_{SW_{MAX}}$) achievable for the TDM can be calculated as $f_{SW_{MAX}} = \frac{1}{t_r} = 15 \div 20kHz$. The switching speed is indeed limited by the cut-off frequency of the setup used to characterize the fabricated die and it will be better estimated in the following (Fig. S11).

To complete the electrical characterization of the superconducting 1I8O demultiplexer, we also evaluated the AC electrical performance. We injected into the signal line I_0-O_4 an AC input current with a 1 kHz frequency, collecting the voltage drop across the line. Figure 5b shows the time-resolved signal line voltages measured by changing the peak-to-peak value of the input current from 2 μA to 16 μA. When the input current instantaneously overcomes the minimum switching current of the JoFETs in the I_0-O_4 path (i.e., I_S = 1.9 μA of

$JoFET_4$), a finite voltage drop is detected. The higher the peak-to-peak value of the input current, the higher the signal line voltage drop obtained.

By applying an AC signal lower than the minimal critical current supported, we then evaluated the electrical behavior of the superconducting 1I8O demultiplexer in the frequency range from 10 kHz to 100 MHz (LF-VHF radio spectrum) in a dilution fridge equipped with a 50Ω-matched cryogenic measurement setup (maximum operation frequency ~300 MHz, Fig. S12). A lock-in amplifier and a vector network analyzer (VNA) were used to measure the magnitude of the forward power gain scattering parameter ($|S_{21}|$) in the 10 kHz – 10 MHz and 300 kHz – 100 MHz ranges, respectively. We simultaneously measured the output powers of signal lines I_0-O_4 and I_0-O_6, injecting an AC input signal with a −80 dBm power level (10 pW, 447 nA_{rms}). Gate settings were chosen to make superconductive only one line at a time. Figure 5c shows the insertion loss ($IL(dB) = -S_{21}(dB)$) of the signal line I_0-O_4 in the dissipative and non-dissipative states. When the signal line is superconducting, an insertion loss of ~0 dB was measured in the whole frequency range, demonstrating that the input power is efficiently transferred to the output port of the selected signal line without significant dissipation along the path. This is a remarkable improvement compared to the case in which the demultiplexer in the ON-state operates above the critical temperature of Al (specifically at 1.65 K) and, therefore, in a fully dissipative configuration. In this case, the insertion loss increases to ~ 5.5 dB (Fig. S13). The latter result highlights the importance of a fully superconducting path between the input and the output port. Compared with conventional gate-tunable cryogenic non-superconducting solutions, it promises a significant competitive advantage of a switchable superconducting system like the one we proposed. On the other hand, when the line is gated in the dissipative state, the insertion loss increases to ~17.5 dB, which is relatively constant over all the frequency range tested and allows to achieve an $\frac{ON}{OFF}$ ratio of ~ 17.5 dB. Similar results were also obtained for the signal line I_0-O_6 (Fig. S14).

The turn-OFF and turn-ON time-resolved behaviors of a typical JoFET (L_{JJ} = 500 nm, W_{JJ} = 4 µm, and L_G = 1000 nm) were reported in Fig. 5d, e. The electrical characterization was performed in a dilution fridge equipped with a very-high-frequency (VHF) measurement setup (cut-off frequency ~ 100 MHz for the gate control lines, cut-off frequency ~ 500 MHz for the drain-to-source signal lines). An AC sinusoidal wave (-80 dBm power and 100 MHz frequency) was used as the drain-to-source signal; a square wave (t_r=t_f ~ 130 ns, Fig. S15) was used as the gate control switching signal. Switching from the ON to OFF state (Fig. 5d), the steady-state peak-to-peak voltage value of the drain-to-source wave reduces by ~7.6 times (17.6 dB in power), according to what reported in Fig. 5c. The increased wave amplitude observed during the transient was related to the displacement current generated during the gate capacitor discharge upon application of the square wave control signal. Specifically, this current sums to the drain-to-source signal current, increasing the value of the drain-to-source wave voltage measured. A similar trend was observed also for the OFF-to-ON state commutation (Fig. 5e). In this case, t_r=t_f ~ 100 ns were achieved and traduced in an improved $f_{SW_{MAX}} = 10MHz$, as demonstrated by the uncorrelation between t_r and t_f and the gate switching frequency reported in Fig. S16. Also in this case, $f_{SW_{MAX}}$ is limited by the cut-off frequency of the setup used to drive the gate control lines of the superconducting demultiplexer (Fig. S15). Figure S17 depicts the AC drain-to-source wave increasing the JoFET gate control switching frequency from 1 kHz to 100 kHz, from which the amplitude of the drain-to-source wave was reliably and reproducibly modulated as a function of the gate voltage value applied in time.

We then theoretically estimated the static (P_{STAT}) and dynamic (P_{DYN}) power dissipated by the 1I8O superconducting demultiplexer. In the DC-to-f_{MAX} range, P_{STAT} is related to the part of the input current flowing in the dissipative OFF branches (see Section 6 of Supporting Information). P_{STAT} ~ 700 fW was evaluated for the superconducting demultiplexer operating in the measurement setup of Fig. 5c and S12. The dynamic power dissipated by the switching activity was calculated by the well-known formula $P_{DYN} = n \times C_G \times V_{GS}^2 \times f_{SW}$, where $n = 14$ is the number of integrated JoFETs, $C_G = C_{GS} + C_{GD}$ is the gate capacitance, and f_{SW} is the gate control switching frequency (see Section 7 of Supporting Information). Referring to the cooling power of the cryostat we used throughout the experiments at the temperature of 50 mK, namely 16 µW, the 1I8O superconducting demultiplexer can operate with control switching frequencies up to 400 kHz without affecting the temperature of the coldest plate. The calculations were performed in the worst-case scenario of the full P_{DYN} dissipated at the mixing chamber stage. The switching frequency can be increased by reducing the size of the JoFETs and the gate voltage required to reach the OFF state.

InAsOI-based µwave superconducting 1-input-2-outputs analog demultiplexer

To envisage TDM of supercurrents in the frequency operational range of transmon qubits, we focused on the development of a µwave superconducting 1-input-to-2-outputs (1I2O) analog demultiplexer operating at 50 mK. The chip was manufactured with the same InAsOI-based technology previously described and features 2 JoFETs ($JoFET_0$ and $JoFET_1$), 1 input line (I_0), 2 output lines (O_0 and O_1), and 2 control lines (G_0 and G_1). On-chip routing of electromagnetic signals in the µwave regime was performed by using integrated Al superconducting coplanar waveguides (CPWs), to minimize power dissipation along the I/O line in the ON-state due to the comparable values of λ_{GaAs} with the dimension of the chip at higher operating frequencies. Figure 6a shows a false-color optical microscope image of the fabricated die, with signal and control lines highlighted in red and blue.

The chip is 6 × 6 mm^2 and embeds two JoFETs with W_{JJ} = 6 µm, L_{JJ} = 800 nm, and L_G = 1000 nm routed with Al CPWs. The gate extension L_G was reduced compared to that of the JoFETs integrated into the 1I8O superconducting demultiplexer to address the gate capacitance limitation on the OFF-state electrical properties at high frequencies, consequently increasing $f_{MAX_{OFF}}$. Both the JoFETs operate as expected, as reported from the I_S and R_N vs. V_{GS} trends depicted in Fig. 6b, from which the full suppression of the switching current as well as ~20 times increase of the normal state resistance was achieved in the gate range 0 to −4.5 V. The behavior of the signal line I_0-O_0 was collected and considered as representative of all the lines of the chip, with gate settings chosen to make superconductive only one signal line at a time (Fig. 6c). An AC signal with amplitude lower than the minimal switching current supported was used to evaluate the electrical behavior of the µwave 1I2O superconducting demultiplexer in the frequency range from 500 MHz to 4 GHz (VHF-UHF radio spectrum) by involving a dilution fridge equipped with a 50Ω-matched cryogenic measurement setup (maximum operation frequency ~ 8.5 GHz, Fig. S18). An electromagnetic wave with power P_{IN} = -80 dBm (10 pW, 447 nA_{rms}) was provided to the input port I_0; the power of the electromagnetic wave reaching the output port O_0 was collected during while the outport port O_1 was connected to a reference load of 50 Ω. Figure 6d shows IL of line I_0O_0 in the non-dissipative and dissipative states. In the non-dissipative state, an IL of 0 dB was observed throughout the frequency range, confirming negligible power consumption along the fully superconducting line in the VHF-UHF radio spectrum range. On the other hand, in the dissipative state, the IL increases to ~16 dB, from which an $\frac{ON}{OFF}$ ratio of 16 dB is calculated. The achieved performance are comparable to what was observed for the 1I8O superconducting demultiplexer chip, which allow us to conclude that the proposed architecture can be employed also for operating TDM of non-dissipative supercurrents in the frequency operational range of transmon qubits. Further considerations on the use of superconducting TDM of non-dissipative signals to transmon qubits for a

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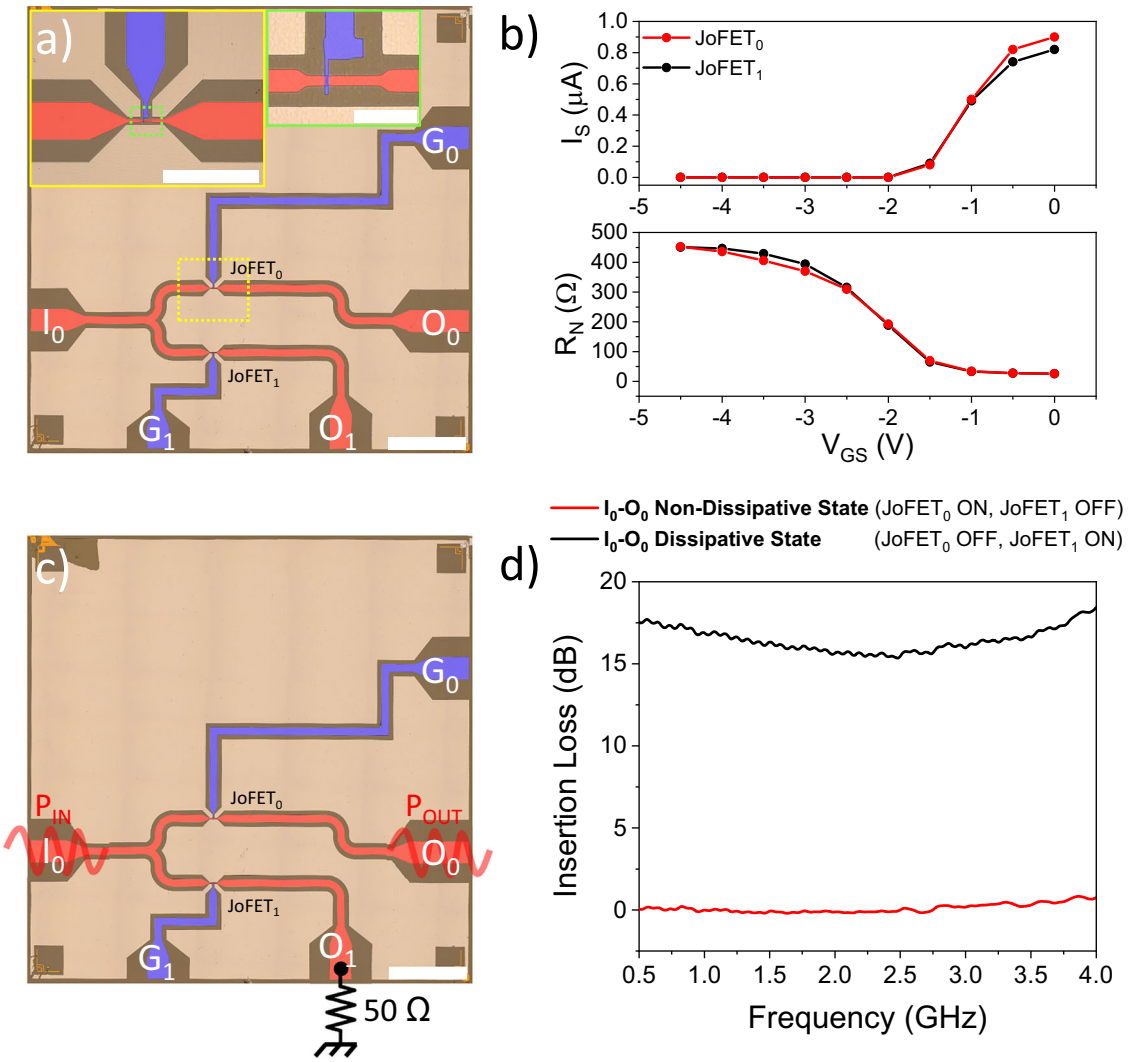


Fig. 6 | Morphological, DC, and RF electrical characterization of the μwave superconducting 1-input-2-outputs analog demultiplexer. a False-color optical microscope image of the μwave superconducting 1I2O demultiplexer; the scalebar is 1 mm. Yellow and green insets report false-color optical microscope image of an integrated JoFET; scalebars are 250 μm and 25 μm, respectively. **b** Downward gate-dependent switching current and normal-state resistance of the integrated JoFETs featuring $W_{JJ} = 6$ μm, $L_{JJ} = 800$ nm, and $L_G = 1000$ nm. **c** False-color optical microscope image of the μwave superconducting 1I2O demultiplexer highlighting the electrical configuration used to test the chip. **d** Frequency-resolved insertion loss of signal line I_0-O_0 in the non-dissipative and dissipative states.

dramatic reduction of the I/O lines of a cryogenic quantum computer are reported in Section 8 of the Supporting Information.

In conclusion, our work introduces a significant technological advancement in the form of TDM of non-dissipative signals with a voltage-actuated hybrid superconducting demultiplexer. This innovative device is designed to substantially reduce the number of input signal lines required in a conventional cryostat. The key component of the demultiplexer is an InAsOI-based JoFET, which features Al as a superconductor and HfO_2 as a gate insulator. Notably, this JoFET has the capability to completely suppress the switching current and increase the normal-state resistance by 20 times when subjected to a gate voltage of −4.5 V. In this context, the ideal building block should be capable of (i) exhibiting a high switching current in the ON-state, (ii) entirely suppressing the switching current in the OFF-state, and (iii) exhibiting a high normal-state resistance in the OFF-state. We manufactured a superconducting demultiplexer with 1 input and 8 outputs exhibiting a significant non-dissipative dynamic input range of $-2 \div 2$ μA and able to operate up to 100 MHz in signal frequency and 100 kHz in switching frequency at 50 mK. The results are remarkable, revealing an insertion loss of approximately 0 dB in the superconducting state and an $\frac{ON}{OFF}$ ratio of approximately 17.5 dB up to 100 MHz in a 50Ω-matched cryogenic measurement setup. These findings vividly illustrate the advantage of superconductivity by establishing a lossless path between the input and output ports. Additionally, the integration of on-chip routing for non-dissipative signals utilizing superconducting coplanar waveguides was employed to expand the operational frequency range of the superconducting demultiplexer. A superconducting demultiplexer with 1 input and 2 outputs was fabricated and validated up to 4 GHz in signal frequency at 50 mK. Also for the latter device, an insertion loss of ~0 dB in the superconducting state and an $\frac{ON}{OFF}$ ratio of ~16 dB were evaluated. These groundbreaking advancements demonstrate the potential for the practical implementation of superconducting TDM, which could substantially reduce in I/O lines, costs, and space occupation within a cryostat.

Methods

All the methods regarding the sample manufacturing and the cryogenic electric characterization are detailed reported within the Supporting Information file.

InAsOI heterostructure growth via molecular beam epitaxy

InAsOI was grown on semi-insulating GaAs (100) substrates using solid-source Molecular Beam Epitaxy. Starting from the GaAs substrate, the sequence of the layer structure includes a 200 nm-thick GaAs layer, a 200 nm-thick GaAs/$Al_{0.16}Ga_{0.84}As$ superlattice, a 200 nm-thick GaAs layer, a 1.250 µm-thick step-graded $In_XAl_{1-X}As$ metamorphic buffer (with X increasing from 0.15 to 0.81), a 400 nm-thick $In_{0.84}Al_{0.16}As$ overshoot layer, and a 100 nm-thick InAs layer. The GaAs layer and GaAs/AlGaAs superlattice are grown at 600 °C ± 5 °C. The metamorphic buffer and the overshoot layers were grown at optimized substrate temperatures of 320 °C ± 5 °C. The InAs epilayer was grown at 480 ± 5 °C.

InAsOI Josephson Field Effect Transistor fabrication

InAsOI substrates were cut into square samples and cleaned with organic solvents. The air-exposed InAs surface was etched from native InAs oxide ($InAsO_X$) and passivated with S-termination by dipping the InAsOI samples in a $(NH_4)_2S_X$ solution (290 mM $(NH_4)_2S$ and 300 mM S in DIW) at 45 °C. The S-terminated InAsOI samples were then rinsed in DIW and loaded into an e-beam evaporator, where a 100-nm-thick Al layer was deposited. After Al deposition, the mesa geometry was defined via photolithography and subsequent Al etching in Al Etchant Type D at 40 °C and InAs etching with a H_3PO_4:H_2O_2 solution (348 mM H_3PO_4, 305 mM H_2O_2 in DIW). After MESA fabrication, nanometric aligning Ti/Au markers were defined via e-beam lithography, thermal deposition of a 10/50-nm-thick Ti/Au bilayer, and lift-off. Markers were then used to define the Josephson Junction via e-beam lithography and subsequent Al etching in Al Etchant Type D at 40 °C. The 31-nm-thick HfO_2 gate insulator layer was deposited via Atomic Layer Deposition at a temperature of 130 °C. Eventually, markers were again used to define the metallic gate via e-beam lithography, e-beam deposition of a 10/100-nm-thick Ti/Al bilayer, and lift-off.

InAsOI superconducting 1I8O demultiplexer fabrication

The superconducting 1I8O demultiplexer chip was fabricated according to the step previously reported for the InAsOI Josephson Field Effect Transistor Fabrication. Photolithography was used as the patterning technique to define the metallic gate lines aligned with micrometric markers fabricated at the mesa stage.

InAsOI µwave superconducting 1I2O demultiplexer fabrication

The µwave superconducting 1I2O demultiplexer chip was fabricated according to the step previously reported for the InAsOI Josephson Field Effect Transistor Fabrication.

Data availability

All the data are available upon request from the corresponding author.

Code availability

No code is used in this study.

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Author contributions

A.P. and F.G. conceptualized the experiments. A.P. and L.S. fabricated the samples. A.P. and S.T. performed the experiments. A.P., L.B., and S.T. analyzed the data. A.P. performed the electrical simulations. A.P. prepared the figures and wrote the original draft. A.P., L.B., S.T., G.D.S., E.S., L.S., and F.G. discussed the results and contributed to the original draft. A.P. led the review process. L.B., E.S., and F.G. contributed to the review process. F.G. supervised the overall activity.

Competing interests

The authors declare no competing interests.

Additional information

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