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Electrostatic Control of the Thermoelectric Figure of Merit in Ion-Gated Nanotransistors

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Semiconductor nanostructures have raised much hope for the implementation of high-performance thermoelectric generators. Indeed, they are expected to make available reduced thermal conductivity without a heavy trade-off on electrical conductivity, a key requirement to optimize the thermoelectric figure of merit. Here, a novel nanodevice architecture is presented in which ionic liquids are employed as thermally-insulating gate dielectrics. These devices allow the field-effect control of electrical transport in suspended semiconducting nanowires in which thermal conductivity can be simultaneously measured using an all-electrical setup. The resulting experimental data on electrical and thermal transport properties taken on individual nanodevices can be combined to extract ZT, guide device optimization and dynamical tuning of the thermoelectric properties.

1. Introduction

Nanoscale heat management is a demanding need for practical nanoelectronics applications owing to the intrinsic link between heat and charge flow. A notable example is CMOS technology where today's extreme operational regimes make managing charge flow and heat dissipation in transistors a huge technological challenge both in conventional rigid[1,2] and flexible[3] devices. Moreover, controlling heat flow at the nanoscale may open the way to the realization of phonon logics, thus introducing a new paradigm for non-electronic devices exploiting harvested energy for operation.[4] Furthermore, recently-developed bioelectronic and wearable devices need environmentally-friendly energy sources and possible game changers may be found in thermoelectric energy harvesters relying on naturally-produced heat to provide energy.[5] For all these applications semiconducting nanowires have attracted much interest owing to their versatility and unique properties such as their high aspect ratio and ease of realization both for homogeneous nanostructures and heterostructures. These properties have made them promising for thermoelectrics[6–9] and nano-electronics,[10–13] as well as iontronic nanodevices,[14–17] optoelectronics,[18,19] sensing[20–22] and quantum computing.[23,24]

In the quest for high-efficiency thermoelectric materials, a relevant parameter to be taken into account is the figure of merit $ZT = \sigma S^2 T/\kappa$, where σ is the electrical conductivity, κ is the thermal conductivity, and S is the material-dependent Seebeck coefficient.[25] The optimization of ZT is usually achieved by following two paths. On one hand thermal conductivity is reduced by employing nanostructured materials—for example, nanowires—whose dimensions are comparable to the phonon mean free path,[26–28] on the other field-effect modulation of the electrical properties is exploited to modulate electrical conductivity and the electronic contribution to the Seebeck coefficient that is, ultimately, the power factor σS^2.[29–34] Measuring thermal transport while simultaneously tuning electric transport on the same nanostructure is a difficult task, owing to different device architectures usually required for the measurement of thermal conductivity (suspended nanostructures) and for electric gating in order to achieve field-effect control of the electrical conductivity (nanostructure must be strongly coupled to the gate and is therefore typically in contact with a gate dielectric).

In this work ionic liquids are exploited as a mean to overcome this problem and allow these simultaneous measurements. In fact, thanks to their liquid nature they naturally wrap around suspended nanostructures thus providing a dielectric medium and yielding access to a highly efficient field effect. At the same time, thanks to their very poor thermal transport properties[35,36] they do not perturb the nanostructure thermal

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conductivity. In this article we experimentally demonstrate a novel concept of ionic-liquid-gated nanowire based electric double-layer transistor (EDLT), that allows us to simultaneously probe electrical and thermal properties of the nanostructure under analysis. As test materials, we focused mostly on n-doped InAs nanowires on the semiconductor side and tetraoctylphosphonium bis(trifluoromethanesulfonyl)imide ([P8888][Tf2N]) on the ionic liquid side. The EDL gating mechanism that we are exploiting features very strong gate coupling, being the gate dielectric conformally surrounding the semiconductor nanostructure. One would expect enhanced gating performance on nanowires featuring lower diameters, since stronger field effect is achievable: this would allow for stronger field effect and overall increased device performance. While this holds in general for semiconductor nanomaterials featuring electrical conduction in the entire body of the nanostructure, InAs specifically is characterized by Fermi pinning in the conduction band due to surface states, which causes charge accumulation in the vicinity of the nanowire interface with the ionic liquid, regardless to the nanowire diameter. Therefore, the degree of modulation of ZT is not expected to change dramatically for InAs nanowires having different diameters.

We show that the measurement of nanowire thermal conductivity is performed together with the modulation of the electrical properties on the same nanostructure. Our data allow us to determine the Seebeck coefficient of the semiconductor and to quantitatively show the field-effect modulation of the thermoelectric figure of merit of the nanowire at room temperature. Finally, in order to demonstrate the generality of our architecture, we implemented it with silicon nanowires and explored device operation with another ionic liquid, that is, 1-ethyl-3-methylimidazolium bis(trifluoromethanesulfonyl) imide ([Emim][Tf2N]), as gate dielectric.

Our results show that our gates do not affect nanowire thermal-conductivity measurements and allow us to modulate the thermoelectric figure of merit in these high-aspect-ratio nanostructures. Perspectives of this work include the possibility to measure and modulate the thermoelectric figure of merit of nanowire-based thermoelectric generators with dynamically optimized performance. Furthermore, the platform developed in this work will enable further studies of the coupling of heat and charge flow at the nanoscale, and provide a testbed for the implementation of nanoscale thermal transistors and heat valves.

2. Results and Discussions

We report field-effect control of the thermoelectric figure of merit for InAs and Si nanowires gated by a phosphonium-based ionic-liquid droplet ([P8888][Tf2N]). Data relative to device operation with a different ionic liquid ([Emim][Tf2N]) will be reported in the Supporting Information (Section SI, Supporting Information): in this latter case experiments yield results fully consistent with those reported in the main text, confirming the efficacy of the present approach irrespectively of the chosen ionic-liquid. Nonetheless, it is worth mentioning that the specific ionic-liquid choice was driven by considerations on electrolyte thermal stability: phosphonium-based ionic liquids are preferable for high temperature applications as is customary in thermoelectric generators (see Section SI, Supporting Information).

2.1. Thermal Conductivity Measurement in InAs Nanowire EDLTs

Nanowire thermal conductivity measurements were previously reported and exploited based both on optical[37,38] and on electrical techniques.[39] The latter allow one to measure the thermal conductivity of single nanostructures while being able to access their electric-transport properties,[40] but have a major drawback when it comes to simultaneously modulate electric transport in the same structure. As mentioned above, this stems from the need to physically detach the nanowire from the substrate in order to avoid thermal losses: the resulting suspended device architectures do not allow field-effect modulation of the electrical conductivity with conventional gating techniques, for example solid-state gates.

The present scheme is designed to allow field-effect conductance modulation together with thermal-conductivity measurements via the 3ω technique.[41] **Figure 1** reports the device architecture for InAs nanowires (scanning electron micrographs in panels (a,b) in Figure 1 and schematic view in panel (c) in Figure 1) together with some details on the device equivalent circuit (panel (d) in Figure 1). The nanowire is thermally anchored at its ends via two metallic contacts (square contacts labeled "I injection" in panel (a) in Figure 1) designed to act simultaneously as ohmic contacts and heat sinks, ensuring a fixed temperature at the nanowire extremities thanks to the very large area of the contact (typically exceeding 10×10 μm^2) together with the high gold thermal conductivity. These thermal-anchoring contacts are used as electrical contacts to inject an AC current I_ω. Two additional contacts (labeled "V probe" in panel (a) in Figure 1) are used to measure the nanowire voltage drop V_ω. The starting point to derive κ is its link to the third harmonic of the voltage drop measured between the inner contacts ($V_{3\omega}$):[41]

$$V_{3\omega} = \frac{4R\alpha L}{\pi^4 \kappa A} I_\omega^3 \tag{1}$$

where R is the nanowire resistance, α is the temperature coefficient of this resistance (i.e., the variation of nanowire resistance with temperature), L is the channel length, A is the section, κ is the thermal conductivity, and I_ω is the amplitude of the injected AC current. The model strictly applies to ideal systems having infinite aspect ratio (i.e., infinitely long and thin wires): its application to real systems with finite aspect ratios requires the use of finite-element modeling (Section SII, Supporting Information). Equation (1) shows that it is possible to evaluate κ for the device under analysis by fitting the functional dependence of $V_{3\omega}$ with respect to the injected current I_ω. An example of such a fit is reported in panel (e) in Figure 1. Moreover, devices are embedded in an ionic liquid droplet—not shown in the scanning electron micrograph—that can be polarized via a counter-electrode, visible in the zoomed-out scanning electron micrograph in panel (b) in Figure 1, to which a DC voltage V_{LG} is applied. This provides

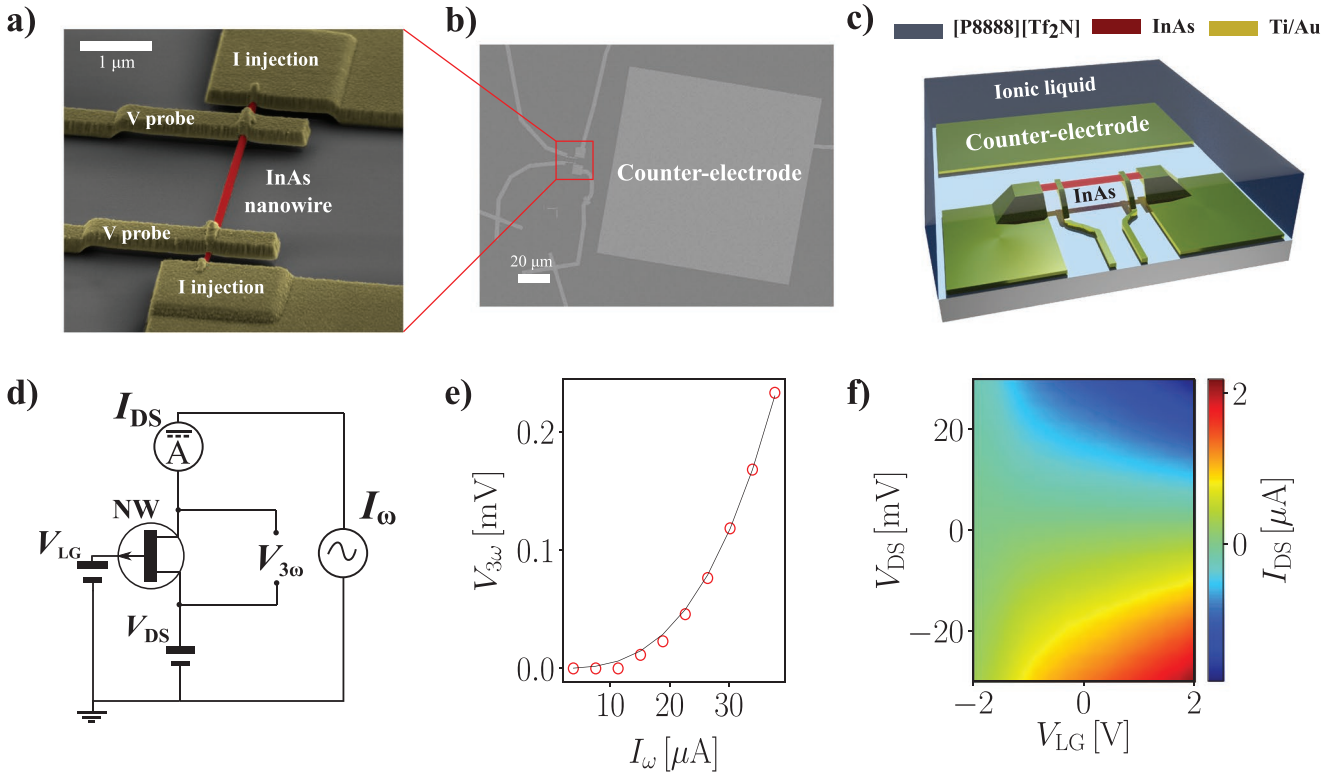

Figure 1. Device architecture and operation for combined electrical and thermal transport measurements. a) False colored tilted scanning electron micrograph of a prototypical suspended InAs nanowire based device. Yellow color is used to highlight gold ohmic contacts, while the InAs nanowire is highlighted in red. b) Zoom-out scanning electron micrograph of the same device. Here, the square counter-electrode used to manage the ionic arrangement in the ionic liquid surrounding the device is visible. c) Device architecture pictorial view and d) equivalent circuital scheme for simultaneous electrical and thermal transport measurements. The entire device is embedded in an ionic liquid droplet - represented by the blue color. Yellow and red are used for the contacts and nanowire, respectively. In order to perform field effect device operation, a voltage V_{LG} is applied to the counter-electrode. DC current measurement are performed by applying a bias voltage V_{DS} between the inner contacts while the current I_{DS} is measured. For the extraction of the thermal conductivity, the nanowire is fed by means of an AC current I_ω and the third harmonic of the voltage drop $V_{3\omega}$ is measured between the inner contacts. e) Typical acquisition of $V_{3\omega}$ versus I_ω (for this acquisition $V_{LG} = 0$). f) DC current measurement with respect to V_{LG} and V_{DS}, reporting n-type semiconducting behavior.

the field-effect control of the electrical conductivity. Panel (f) in Figure 1 reports a DC current measurement performed by applying a DC voltage bias V_{DS} between the inner contacts of the nanowire and the counter-electrode voltage V_{LG}. The same I–V characteristic can be extracted by employing either the first harmonic of the voltage drop in the nanowire or DC measurements: the result was found to be fully consistent. Here, the current I_{DS} flowing through the active channel is measured and the expected n-type semiconducting behavior is visible.

Figure 2 reports our results for the measurement of thermal conductivity at different counter-electrode voltages for a [P8888][Tf2N]-gated InAs nanowire EDLT. Panel (a) in Figure 2 reports the measured third harmonic of the voltage drop ($V_{3\omega}$) as a function of the injection current I_ω for several applied counter-electrode voltages. The resistance of the channel was readily obtained by measuring the first harmonic of the voltage drop: it is reported of Figure 2b. For what concerns α, that is the temperature coefficient of resistance, it was obtained on the same device by measuring the resistance of the active channel while heating up the device. The measurements reported in Figure 2 were performed with an injection frequency $f = 8$ Hz, on a nanowire with $L = 2331$ nm and diameter $D = 150$ nm.

The resulting thermal-conductivity values of the InAs nanowire are reported in Figure 2d for different values of counter-electrode voltage (i.e., for different values of channel conductance that was modulated by field-effect driven by the ionic distribution in the liquid). Values are found to spread within measurement uncertainty, the mean value is $\kappa = 14.2 \pm 0.4$ mW mK^{-1}. Our result is in line with the one reported by other groups using different techniques on InAs nanowires with comparable diameters.[42] This confirms that even if the ionic liquid is able to modulate the resistance of the active channel, it acts as a thermal insulator and allows one to measure the intrinsic nanowire value of κ irrespectively of the applied counter-electrode voltage. In order to further test functionality and limits of operation of the present architecture, we performed thermal conductivity measurements using another ionic liquid. As reported in the Supporting Information, we repeated the measurements on an [Emim][Tf2N]-gated suspended InAs-nanowire EDLT (Section SI, Supporting Information). We found similar phenomenology and results, despite the fact that [Emim][Tf2N] is not specifically designed for operation at high temperatures and is probably not the most efficient gate medium for materials undergoing strong self-heating during

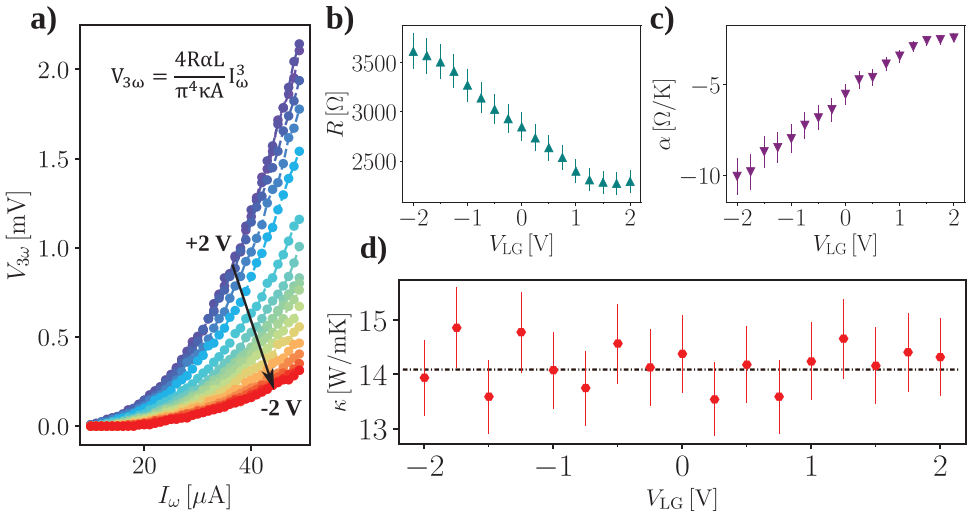

Figure 2. Gate voltage dependence of electronic and thermal transport. a) $V_{3\omega}$ versus I_ω for several values of applied counter-electrode voltage. The curves are fitted by employing both the analytic formula reported in the panel and finite element analysis. The results are combined with the values of the electrical resistance and the resistance temperature coefficient - R and α - reported in (b) and (c), respectively in order to extract the thermal conductivity of the nanowire for each value of applied counter-electrode voltage. d) Thermal conductivity measured for different V_{LG} values. The value for κ roughly oscillates around a mean value which is compatible with values reported in literature.[42]

device operation (i.e., high resistivity materials). Indeed, this suggests that the present architecture is robust toward changes in the employed materials, provided some fundamental conditions are met - for example the ionic-liquid thermal conductivity must be sufficiently lower (typically a factor 100) than that of the semiconductor.

2.2. Electrostatic Control of the Thermoelectric Figure of Merit

We further push the functionality of our platform by extracting valuable parameters allowing us to assess the thermoelectric performance of the nanowire. That is, by using datasets acquired simultaneously on the same nanowire, we can evaluate the thermoelectric figure of merit $ZT = \sigma S^2 T/\kappa$. To date, a few works targeted the gate control of the power factor, without providing any estimation of ZT due to the measurement of the thermal conductivity being inaccessible. For instance, this approach was attempted for carbon nanotubes[34] and silicon nanowires,[30] and power factor calculated modulations comparable to the one observed in our work were reported. The present work reports the field effect modulation of ZT in a nanowire achieved experimentally by varying the electronic conductivity while measuring and keeping under control the thermal conductivity in the same nanowire, ascertaining that thermal conductivity is very small in the nanostructure and remains small during the modulation process. Moreover, while a ZT exceeding one is usually regarded as the threshold for a thermoelectric generator technology to be game changer in real applications, our strategy ensuring a factor ≈1.5 enhancement of ZT is potentially effective, irrespectively of the starting point for the value of the Seebeck coefficient. We evaluate the Seebeck coeffcient S by exploiting the Stratton formula for n-doped semiconductors:

$$S = -\frac{k_b}{e}\left[\frac{5}{2} - \log\left(\frac{n}{N_c}\right)\right] \tag{2}$$

where k_b is the Boltzmann constant, e is the elemental charge, n is the conduction electron density in the semiconductor and N_c is the effective density of states of the conduction band, which is evaluated analytically as follows:

$$N_c = 2\left(\frac{2\pi k_b T m_e^*}{h^2}\right)^{3/2} \tag{3}$$

In this latter formula, T is the temperature and m_e^* is the electron effective mass of the semiconductor under analysis. Thus, in order to evaluate the Seebeck coefficient one must have information about the electronic density n that can be readily estimated from the electrical transport measurements within the Drude model.

Figure 3 shows the dependence on the counter-electrode voltage for each quantity entering the evaluation of ZT relatively to the specific device under analysis. Panels (a–c) in Figure 3 report the electrical conductivity, Seebeck coefficient and the power factor (i.e., σS^2) respectively, while the dependence on the counter-electrode voltage of ZT is reported in panel (d) in Figure 3.

Our results show that it is possible to drive electrostatic modulation of the thermoelectric figure of merit by sweeping the counter-electrode voltage. This is made possible by the present device architecture and in particular by the use of the ionic-liquid gating. With conventional approaches the needed input data need to be extracted from different devices thus introducing an additional uncertainty due to unavoidable sample-to-sample variability. Importantly, the possibility to tune the thermoelectric efficiency may be a powerful degree of freedom for the implementation of thermocouples and other thermoelectric devices. In fact, it would introduce the possibility to dynamically tune the efficiency of individual elements in order to maximize the efficiency of thermoelectric generator arrays.

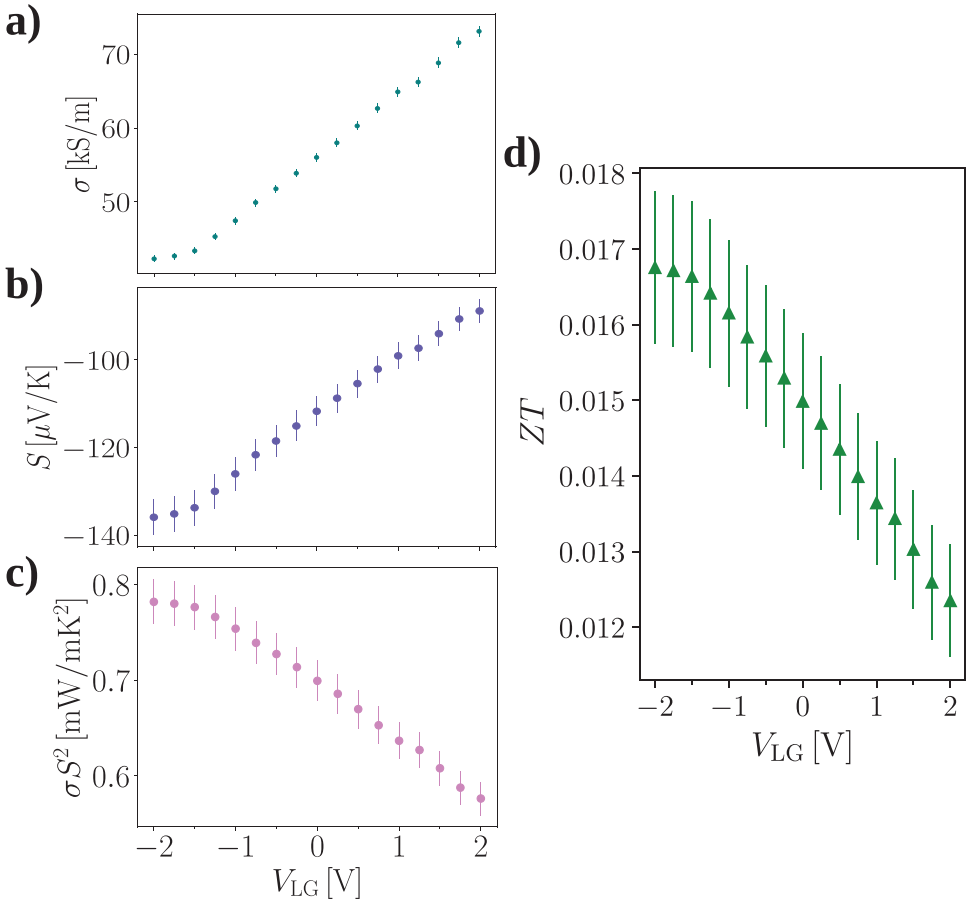

Figure 3. Complete benchmark and electrostatic control over the thermoelectric efficiency. a) Measured electrical conductivity, b) Seebeck coefficient, and c) power factor dependence on the applied counter-electrode voltage. These are combined with the extracted thermal conductivity in order to evaluate the d) thermoelectric figure of merit of the material ZT, which is modulated by V_{LG} in a completely reversible and controllable way ($T \approx 300$ K).

We should like to stress that our data are taken in the temperature regime of interest for practical applications, that is, room temperature and above. At low temperatures it is likely that the value of κ is not constant at different counter-electrode voltages, since the electronic contribution to thermal conductivity is stronger than phononic contribution (i.e., $\kappa_{el} \gg \kappa_{ph}$, contrarily to what happens at room temperature).

2.3. Si Nanowire Figure of Merit Modulation

In order to demonstrate the generality of our approach across different material platforms and fabrication paradigms, we realized devices based on top-down fabricated n-doped Si nanowires. These belong to a class of nanostructures with an opposite paradigmatic approach to InAs nanowires, which are bottom–up grown and dropcasted on the fabrication substrate after being detached from the growth substrate. An example of realized device is shown in the scanning electron micrographs in **Figure 4**a,b, as well as in panel (c) of the same figure, where a pictorial representation of the device is reported. Figure 4 also reports the operation of devices for electrical conductivity modulation, thermal conductivity measurement, as well as thermoelectric figure of merit field effect modulation. Panel (d) in Figure 4 shows the measurement for the thermal conductivity of Si nanowires by exploiting the 3ω technique already exploited above. The ionic liquid used as gate medium is [P8888][Tf2N]. The measured value of κ roughly oscillates around the mean value of $\kappa = 110 \pm 10$ WmK^{-1} and is compatible with values reported in the literature.[43,44] Panels (e–f) in Figure 4 report the dependence of the electrical conductivity and Seebeck coefficient on the applied counter-electrode voltage, respectively. Combining these quantities, it is possible to evaluate the dependence of the thermoelectric figure of merit of the Si nanowire with respect to the counter-electrode voltage (see panel (g) in Figure 4).

Interestingly, in Si nanowires ZT increases with counter-electrode voltage, the opposite behavior to that observed with InAs nanowires. This is due to the interplay of σ and S that enter ZT via the power factor σS^2. As a matter of fact, our fabricated Si nanowires show higher absolute values for the Seebeck coefficient and lower electrical conductivity with respect to InAs nanowires. Since the Seebeck coefficient of n-doped semiconductors is negative and decreases with increasing counter-electrode voltage, the product σS^2 exhibits the reported increasing trend with the counter-electrode voltage.

These results show that the developed approach for the modulation and measurement of the thermoelectric figure

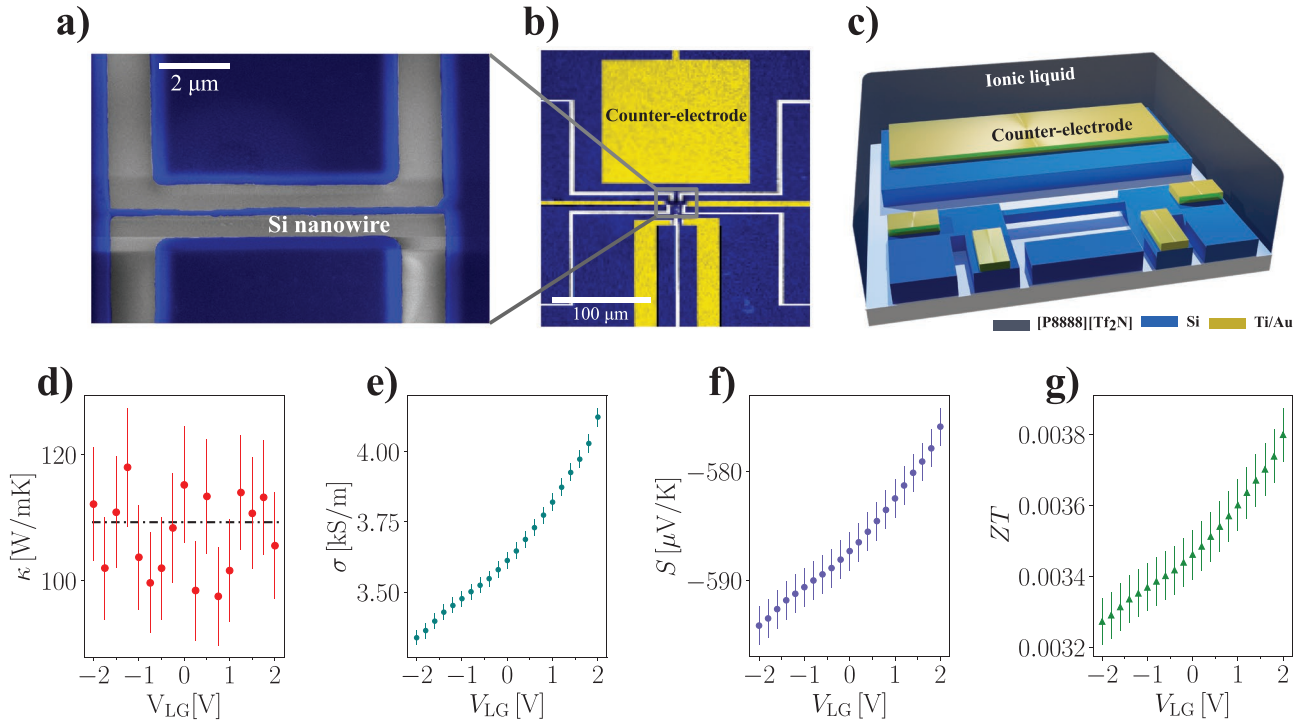

Figure 4. Benchmark and modulation of the thermoelectric efficiency on top–down fabricated Si-nanowire based devices. a) False colored scanning electron micrograph of a prototypical Si nanowire-based device. b) Zoom-out false colored scanning electron micrograph. Blue color highlights silicon, while yellow is used for gold. The counter-electrode used to perform ionic liquid gating is visible. c) Pictorial device representation. The Si nanowire is etched starting from a silicon on insulator substrate and is suspended ≈50 nm over the substrate. Gold contacts are evaporated on the non-etched bulk Si surrounding the nanowire. d) Thermal conductivity, e) electrical conductivity, and f) Seebeck coefficient for one of the tested devices. These quantities are simultaneously measured and allow for the benchmark of the g) thermoelectric figure of merit ZT of the Si nanowire, which is found to be modulated by means of the ionic liquid gate.

of merit of high aspect ratio material is independent of the specific material under analysis and may thus be generally employed. Nonetheless, further improvements may be implemented in our approach in future works. For example, novel ionic liquids may be designed, allowing for stronger gate coupling with the nanostructure which will provide stronger field effect modulation of the electrical properties of the semiconductor and, ultimately, stronger modulation of the thermoelectric figure of merit.

3. Conclusions

We developed a novel device architecture that allows for the first time to monitor and modulate the thermoelectric figure of merit ZT on an individual nanostructure via an all-electrical technique. By combining soft-matter gating with conventional solid-state electronics, we performed thermal conductivity measurements on a device featuring a liquid gate implemented with ionic liquids. The latter excellently perform as gate dielectrics, allowing electrical-conductivity modulation on highly-doped semiconductor nanowires, while acting as thermal insulators. We tested this architecture with different nanowire materials and ionic liquids, finding fully consistent results and device functionalities. We also exploited this functionality to extract the dependence of the thermoelectric figure of merit of a single semiconductor nanowire on the counter-electrode voltage by measuring relevant quantities simultaneously, without having to rely on measurements performed on separate nanowires.

The present device architecture features complete generality toward thermoelectric materials under analysis and can be exploited for the dynamical tuning of the thermoelectric properties of any high aspect-ratio semiconductor. We believe that this work may open the way to the realization of ion-gated thermoelectric generators in which the energy extraction efficiency can be dynamically tuned to ensure optimal performance in varying environmental conditions. Moreover, the inherent flexibility of the employed electrolytes ensures full compatibility with the novel flexible polymeric thermoelectric materials.

4. Experimental Section

InAs Nanowire Device Fabrication: N-type InAs nanowires were grown by gold nanoparticle assisted chemical beam epitaxy (CBE).[45] Typical nanowire length and diameter were 4 μm and 150 nm. The device fabrication protocol started with a sacrificial 200 nm PMMA layer spun on Si++/SiO_2 substrates (0.5 mm Si, 280 nm SiO_2) on which nanowires were drop-casted. The resist under the nanowires was crosslinked by means of electron-beam lithography (EBL) and the unexposed PMMA was removed with acetone followed by an isopropanol rinse. A second EBL step was performed in order to define the metal-electrode patterns on the nanowire and the counter-electrode used to control the ionic distribution in the ionic liquid. A Ti/Au (10/100 nm) bilayer was typically evaporated on the EBL-defined patters in order to define metallic leads

of the devices. Before contact metallization, the nanowire surface was passivated by means of a standard ($(NH_4)_2S_x$ 2% wt in H_2O) solution. Wet chemical etching and passivation in highly diluted $(NH_4)_2S_x$-water solution of the contact area was a standard treatment for obtaining ohmic metal contacts in InAs nanowires. The process selectively etched the native oxide and left a sulfur terminated surface consisting of a disordered chemisorbed sulfur layer on top the semiconductor. Sulfur terminated InAs surface were relatively unstable, but the samples could be exposed to air for a short time, without detrimental effects, which was necessary for transporting and loading the sample in the evaporator vacuum chamber. In this specific case a 2% $(NH_4)_2S_x$ solution was used. After lift-off the crosslinked PMMA underlying the devices was removed by means of oxygen-plasma dry etching (100 W, 100 mTorr, 60 s). In this way the nanostructure was thermally decoupled from the substrate. Four devices were measured in this experiment. For each device, at least two equivalent datasets were generated and analyzed. Then it was proceeded to wire-bond the device to commercial dual-inline packages and then a droplet of ionic liquid was applied on the device prior to measurements.

Si Nanowire Device Fabrication: 1×1 cm^2 wide silicon chips were cleaved from a silicon-on-insulator wafer (260 nm top silicon layer, resistivity 10 Ω cm^{-1}, <100> direction). The chips were doped with phosphorus by thermal diffusion through solid phase: silicon chips were placed in a rapid thermal annealer, in contact with a solid ceramic source, and a pre-deposition step was performed (800 °C, 10 m). A top silicon dioxide layer 50 nm thick was grown by rapid thermal oxidation (1150 °C, 10 m). This second thermal step yielded a uniform distribution of the *n* doping in the top silicon layer with a concentration of about 10^{18} cm^{-3}. Two layers of PMMA (3% in anisole) with different molecular weights were subsequently spun on the chips, to be used as resist for the high-resolution EBL step. After exposure and resist development, an etching of the exposed silicon dioxide by buffered HF for 2 min was performed to transfer the designed geometry onto the oxide layer. The double PMMA layer was then removed by acetone, chips rinsed in isopropyl alcohol, and blow dried with pure nitrogen. The resulting dioxide mask was used to transfer the geometry to the silicon top layer through a KOH etching (35% KOH in water, etch time 7 min at 43 °C). This resulted in a trapezoidal shape of the nanowires with a cross section of 0.1 μm^2. A double layer of PMMA (996k top layer, 350k bottom layer, both 6% in anisole) was then spun on the chips, and a low-resolution EBL step was used to define contacts and connecting leads. After e-beam exposure, 20 nm Cr and 90 nm Au were thermally evaporated, and lift off was performed in hot acetone. Finally, in order to suspend the nanowire and avoid thermal coupling between the nanostructure and the substrate, the buried oxide under the nanowire was removed with a 4 min buffered-HF etching. Two devices were measured in this experiment. For each device, at least two equivalent datasets were generated and analyzed. Following the same procedure as for the InAs nanowires, the devices were wire-bonded to commercial dual-inline packages and then a droplet of ionic liquid was applied.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrolyte gating, semiconductor nanowires, thermoelectrics, thermoelectric figure of merit

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